



AVIT
AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY



VINAYAKA MISSION'S
RESEARCH FOUNDATION
(Deemed to be University under section 3 of the UGC Act 1956)



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION

ENGINEERING

- The research centre setup in the Department focuses primarily to conduct high quality research in state of the art areas such as **cyber security, hardware security solutions** for strategic organizations like **DRDO, ISRO**.
- The Centre has successfully completed the funded project sponsored by Defence Research Development Centre-SAG, Delhi titled “Comprehensive study on Hardware Trojans- Challenges and solutions”.
- Our mission is to develop secure information infrastructures in design and test reliable “TRUSTED PLATFORM MODULE” and other projects related to **hardware security**.
- Currently faculty and students are working on FPGA based design and implementation through HDL Programming and testing in FPGA platform.

Innovation:

- The Department received funding for an amount of **Rs. 9.9475 lakhs** from **DRDO-SAG** for the project Titled “A Comprehensive Study on Hardware Trojans- Challenges and Solutions” on 31.12.2018.
- A final year student participated in **IEEE Students Projects Scheme** and **won cash award of Rs. 5,000** by using this resource.
- Student involved in **AICTE-Chhattra Viswakarma Award** received a fund of **Rs.5,000**.
- **Dr.L.K. Hema**, Professor & HOD received “**Best Researcher Award**” and a cash award of **Rs. 50,000/- from Honorable Chancellor, VMRF**.
- The Department Conducted 1 National Conferences & 2 International Conferences on the theme of VLSI, Embedded Systems, Signal Processing and Communication Technologies (ICVESCO, NCHS'20, ICRESEARCH-2021) from 2018 to 2021 with funding from CSIR, DRDO, BRNS, TNSCST, IEEE, BES, and IETE. This research centre is helping many students to make innovative projects.
- Submitted a project proposal titled “Indigenously designed and fabricated Trusted Platform Module ASIC” for strategic applications in 2019.
- Ms. Pooja Lall & Mr. Gopalakrishnan have done their UG project “Secure hardware implementation of crypto primitives” at SETS lab in 2019.
- An UG project titled “Design and implementation of 4 -2 comparator for multiplier applications” has been completed and communicated for journal publication.

HOD/ ECE



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- Conducted a national level workshop on Hardware security primitives on 20th & 21st June 2021.
- Submitted a project proposal to TNSCST –STPS titled “Hardware security based primitive for vehicles” by Mr. J Vijay , and Mrs. V Vanitha, Assistant Professor, Gr.-II in 2020.
- Design and development of a IOT Based data logger devic for COVID 10. This Project Idea has been submitted to National innovation contest 2020 and went through 2nd rounds and same is applied for Patent in 2021.

HOD/ ECE