AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY
OMR, PAIYANOOR, CHENNAI - 603104
VINAYAKA MISSION'S RESEARCH FOUNDATION
(Deemed to be University under section 3 of the UGC Act 1956)
Accredited by NAAC
Approved by AICTE

**VINAYAKA MISSIONS RESEARCH FOUNDATION**

**AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY, PAIYANOOR**

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**TIMETABLE FOR DSP LAB**

**Ref. No. AVIT / TT / 03**

SEMESTER: **EVEN** ACADEMIC YEAR : **2020-2021**

DEPARTMENT: **ECE** With Effect From: 2**2.02.2021**

| Day/ Period | 1 | 2 | MORNING BREAK ( 11:00-11:15 ) | 3 | LUNCH BREAK (12.15 P.M. - 1.00 P.M.) | 4 | 5 | AFTERNOON BREAK ( 2:55-3.05 ) | 6 |
|---|---|---|---|---|---|---|---|---|---|
| | 9:00-10.00 | 10.00-11.00 | | 11.15- 12.15 | | 1:00-2:00 | 2.00 - 2.55 | | 3.05-4.00 |
| Monday | | | | | | | | | |
| Tuesday | | | | | | | | | |
| Wednesday | | | | | | | | | |
| Thursday | | | | | | | | | |
| Friday | | | | | | | FSD LAB | | FSD LAB |

| Sl.No. | MNEMONIC | COURE CODE | COURSE TITLE | NAME OF THE FACULTY |
|---|---|---|---|---|
| 1 | FSD LAB | 17ECCC90 | FPGA SYSTEM DESIGN LAB | Mr. RAJAT KUMAR DWIBEDI |

**NAME OF LAB. INCHARGE : Mr R Karthikeyan**

HOD/ ECE