AVIT AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY | VINAYAKA MISSION'S RESEARCH FOUNDATION (Deemed to be University under section 3 of the UGC Act 1956) | Accredited by NAAC | Approved by AICTE

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PROG, BRANCH,	**B. E., E. C. E**
YEAR, SEMESTER, SECTION	**III / VI, -**
SUBJECT	**17ECCC90 - FPGA SYSTEM DESIGN LAB**
ACADEMIC YEAR	**2020-2021 (EVEN SEMESTER)**

FPGA SYSTEM DESIGN LAB
STANDARD OPERATING PROCEDURE

Name of the Lab./facility	**FPGA SYSTEM DESIGN LAB**
Purpose	To provide training for students, research scholars and industrial personnel, in response testing digital simulation and analyzing the report.
Scope	Learn Hardware Descriptive Language (Verilog/VHDL), fundamental principles of VLSI circuit design in digital & analog domain, fusing of logical modules on FPGAs, hands on design experience with professional design (EDA) platforms and Design, Simulate and Extract the layouts of Analog IC Blocks using EDA tools.
Responsibility	Faculty In-charge of the facility, HOD/ECE

STANDARD OPERATING PROCEDURE FOR Xilinx

Software tools required:

Synthesis tool: Xilinx ISE 8.2
Simulation tool: Project Navigator
FPGA KIT

PROCEDURE:

- Define the specifications and initialize the design.
- Declare the name of the entity and architecture by using Verilog source code.
- Write the source code in VERILOG.
- Check the syntax and debug the errors if found, obtain the synthesis report.
- Verify the output by simulating the source code.

HOD/ ECE

- Write all possible combinations of input using the test bench.
- Obtain the place and route report.

PRECAUTIONS TO BE FOLLOWED

- Short circuit of the battery terminals or any source terminals has to be avoided.
- Use only shielded probes. Never allow your fingers to slip down to the metal probe tip when the probe is in contact with a hot circuit.

RECORD TO BE MAINTAINED

- Laboratory Manual containing the experiments that can be performed with the personal computer and Xilinx kit.

HOD/ ECE