VINAYAKA MISSIONS UNIVERSITY, SALEM
TAMILNADU, INDIA.

FACULTY OF ENGINEERING & TECHNOLOGY
SCHOOL OF ELECTRONIC SCIENCES
M.E- EMBEDDED SYSTEM TECHNOLOGY
PART TIME
AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY, PAIYANOOR
&
V.M.K.V. ENGINEERING COLLEGE, SALEM
CHOICE BASED CREDIT SYSTEM

2015 REGULATION
# I SEMESTER

<table>
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<tr>
<th>S.No.</th>
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# II SEMESTER

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ME EST R 2015
# IV SEMESTER

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ME EST R 2015
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ME EST R 2015
AIM:

Mathematics is fundamental for any field of technology. The aim of the subject is to impart essential mathematical topics for the PG courses in Electronics and Communication Engineering Department.

OBJECTIVE:

- To understand the concepts of fuzzy logic.
- To make the student learn different matrix methods and some of the applications.
- To understand the concepts of random variables.
- To make the student learn dynamic programming and their applications.
- To understand the concepts of different queuing models.

UNIT I: FUZZY LOGIC

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II: MATRIX THEORY


UNIT III: ONE DIMENSIONAL RANDOM VARIABLES

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform,

Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV: DYNAMIC PROGRAMMING


UNIT V: QUEUEING MODELS


TUTORIAL: 15 HOURS
TOTAL: 60 HOURS
REFERENCES:

AIM:

Learning design of digital circuits is a fundamental necessity for designing embedded systems. This subject provides necessary instruments to achieve that goal.

OBJECTIVE:

To make the student learn: theory of logic and logic functions, design of digital circuits, and an introduction to VHDL language.

UNIT I: ADVANCED TOPICS IN BOOLEAN ALGEBRA 9
Shannon's expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT / INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

UNIT II: THRESHOLD LOGIC 9
Linear separability, Unateness, Physical implementation, Dual comparability, reduced functions, various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

UNIT III: SYMMETRIC FUNCTIONS 9
Elementary symmetric functions, partially symmetric and totally symmetric functions, Mc Cluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

UNIT IV: SEQUENTIAL LOGIC CIRCUITS 9
Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

UNIT V: PROGRAMMABLE LOGIC DEVICES 9
Basic concepts, Programming technologies, Programmable Logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Structure of Standard PLD's, Complex PLD's (CPLD), System Design Using PLD's - Design of combinational and sequential circuits using PLD's, Programming PAL device using PALASM, Design of state machine using Algorithmic State Machines (ASM) chart as a design tool. Introduction To Field Programmable Gate Arrays - Types of FPGA, Xilinx XC3000 series, Logic Cell array (LCA), Configurable Logic Blocks (CLB) Input/Output Block (IOB)- Programmable Interconnect Point (PIP), Introduction to Actel ACT2 family and Xilinx XC4000 families, Design examples.

TOTAL: 45 HOURS
REFERENCES:

AIM:

The use of real time operating systems has become a necessity to build complex embedded systems, this subject is provided.

OBJECTIVE:
To make the student learn fundamentals of Operating Systems, implementation aspects of real time concepts and few applications on RTOS.

UNIT I: REVIEW OF OPERATING SYSTEMS 9


UNIT II: OVERVIEW OF RTOS 9

RTOS Task and Task state - Process Synchronisation- Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronisation problem – Deadlocks -

UNIT I II: REAL TIME MODELS AND LANGUAGES 9

Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT I V: REAL TIME KERNEL 9


UNIT V: RTOS APPLICATION DOMAINS 9


TOTAL: 45 HOURS

REFERENCES:

AIM:

This course aims to give the knowledge for students on all aspects of the design and development of an embedded system, including hardware and embedded software development.

OBJECTIVE:

At the end of this course the student can utilizes and applies the skills and knowledge upon embedded hardware as well as software development.

UNIT I: EMBEDDED DESIGN LIFE CYCLE


UNIT II: PARTITIONING DECISION


UNIT III: INTERRUPT SERVICE ROUTINES

Watch dog timers – Flash Memory basic toolset – Host based debugging – Remote debugging – ROM emulators – Logic analyser – Caches – Computer optimisation – Statistical profiling

UNIT IV: IN CIRCUIT EMULATORS


UNIT V: TESTING


TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

ME EST R 2015
REFERENCES:

AIM:
To introduce concepts of data communication networks.

OBJECTIVE:
To make the student learn, all parts of communication software in layered architecture.

UNIT I OVERVIEW OF COMPUTER NETWORKS AND APPLICATION LAYER PROTOCOLS 9
An introduction to internet - An overview of circuit switching - Packet switching and message switching - Routing in data networks - Access networks and physical media - Protocol; layers - Comparison of OSI and Internet protocol stack - Internet backbones - Network access points and ISPS, Application layer protocols - Service provided by the Internet transport protocols – Network applications: www - Overview of HTTP - HTTP message format - User server interaction – Web caches FTP - FTP commands and replies - Electronic mail in the internet - SMPT, MIME – Mail access protocols - POP3 DNS - Introduction to socket programming with TCP and UDP.

UNIT II TRANSPORT LAYER PROTOCOLS 9
Transport layer services and principles - Relationship between transport and network layers - Overview of transport layer in the internet - Multiplexing and demultiplexing applications connectionless and connection oriented transports - Principles of reliable data transfer – Principles of congestion control.

UNIT III NETWORK LAYER 9

UNIT IV DATA LINK AND MAC LAYER 9
Data link layer services and adapters - Error detection and correction techniques – Multiple Access protocols and LANs - LAN addresses and ARP - Ethernet - Hubs - Bridges and Switches PPP- ATM-X.2.5 and Frame relay.
UNIT V NETWORK SECURITY AND MULTIMEDIA

Networks security - Principles of cryptography - Authentication - Integrity - Key distribution and certification - Secure Email - Internet commerce - Network layer security - Multimedia networking application - Streaming stored audio and video - Internet phone - Case study - RTP.

TOTAL: 45 HOURS

REFERENCES

3. T.N.Saadavi,M.H.Ammar & AL . Halleem” Fundamentals of Telecommunication Networks “ -
LIST OF EXPERIMENTS

1. Design with 8 bit Microcontrollers 8051/PIC Microcontrollers
   i) I/O Programming, Timers, Interrupts, Serial port programming
   ii) PWM Generation, Motor Control, ADC/DAC, LCD and RTC Interfacing, Sensor Interfacing
   iii) Both Assembly and C programming
2. Design with 16 bit processors
   I/O programming, Timers, Interrupts, Serial Communication,
3. Design with ARM Processors.
   I/O programming, ADC/DAC, Timers, Interrupts,
4. Study of one type of Real Time Operating Systems (RTOS)
5. Electronic Circuit Design of sequential, combinational digital circuits using CAD Tools
6. Simulation of digital controllers using MATLAB/LabVIEW.
7. Programming with DSP processors for
   Correlation, Convolution, Arithmetic adder, Multiplier, Design of Filters - FIR based , IIR based
8. Design with Programmable Logic Devices using Xilinx/Altera FPGA and CPLD
   Design and Implementation of simple Combinational/Sequential Circuits
9. Network Simulators
   Simple wired/ wireless network simulation using NS2

TOTAL: 30 HOURS

REFERENCES:

3. Jan Axelson ‘Embedded Ethernet and Internet Complete’, Penram publications

ME EST R 2015
AIM:
Any Embedded design mostly involves processor systems, this course describes computer architectures.

OBJECTIVES:
- At the end of this course the student will know various parallel processing applications and their performance towards real time computing.
- To impart knowledge on scalable architectures and the performances.

UNIT I- THEORY OF PARALLELISM, PARTITIONING AND SCHEDULING  
Parallel Computer models: The state of computing, Multiprocessors and Multicomputers, Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks. Program and network properties: Conditions of parallelism, Program partitioning and scheduling, program flow mechanisms, System interconnect architectures.

UNIT II- SCALABLE PERFORMANCES & HARDWARE TECHNOLOGIES  

UNIT III- MEMORY ORGANIZATIONS & PIPELINING  
Bus cache and shared memory: backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models. Pipelining: Linear and non-Linear Pipeline processors-Instruction pipeline design and Arithmetic pipeline design.

UNIT IV- PARALLEL & SCALABLE ARCHITECTURES  
Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V-SOFTWARE & PARALLEL PROCESSING  
Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL: 45 HOURS

TEXT BOOKS:

REFERENCE BOOKS:
AIM:

To introduce some C concepts relevant to embedded systems with 80x86 family as basis and UML.

OBJECTIVE:

To make the student learn: use of C language for embedded applications, real time UML concepts, co-design methods.

UNIT I  LOW LEVEL PROGRAMMING IN C  9


UNIT II  C AND ASSEMBLY  9


UNIT III  OBJECT-ORIENTED ANALYSIS AND DESIGN  9


UNIT IV  UNIFIED MODELLING LANGUAGE  9


UNIT V  CASE STUDIES  9


TUTORIAL: 15 HOURS
REFERENCES:

2. Hassan Gomma, “Designing Concurrent, Distributed, and Real-Time applications with UML.
AIM:
This course will introduce approaches and methodologies for VLSI architectures of signal processing.

OBJECTIVE:
- At the end of this course the student can have knowledge about the basic approaches and methodologies for VLSI architectures of signal processing.
- The students will also have hands-on VLSI system design experience using hardware description language (HDL) and commercial EDA tools (Synopsys).

UNIT I  INTRODUCTION  9
Overview of digital VLSI design methodologies - Trends in IC technology – advanced Boolean algebra - Shannon’s expansion theorem - consensus theorem - Octal designation - Run measure - Buffer gates - Gate Expander - Reed Muller expansion - Synthesis of multiple output combinational logic circuits by product map method - Design of static hazard free and dynamic hazard free logic circuits.

UNIT II  ANALOG VLSI AND HIGH SPEED VLSI  9
Introduction to analog VLSI - Realisation of Neural networks and switched capacitor filters - sub-micron technology and GaAs VLSI technology.

UNIT III  PROGRAMMABLE ASICS  9
Anti fuse – static RAM – EPROM and EEPROM technology - PREP bench marks –Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC & AC inputs and outputs-clock and power inputs - Xilinx I/O blocks.

UNIT IV  PROGRAMMABLE ASIC DESIGN SOFTWARE  9

UNIT V  LOGIC SYNTHESIS, SIMULATION AND TESTING  9
Basic features of VHDL language for behavioural modelling and simulation - Summary of VHDL data types – dataflow and structural modelling – VHDL and logic synthesis – types of simulation – boundary scan test-fault simulation – automatic test pattern generation

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

ME EST R 2015
REFERENCES:

2. Amar Mukherjee, Introduction to NMOS and CMOS VLSI system design, Prentice hall 1986

ME EST R 2015
AIM:
This course aims to provide students with an understanding of digital image processing techniques, including image reconstruction and restoration, segmentation and enhancement, also colour and morphological image processing techniques.

OBJECTIVE:
Upon successful completion of this course, students should be able to understand all types of image processing techniques.

UNIT I: INTRODUCTION TO IMAGE PROCESSING SYSTEMS & IMAGETRANSFORMS 9

Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Applications of Digital image processing

Introduction, Need for transform, Image transforms, Fourier transform, 2 D Discrete Fourier transform and its transforms, Importance of phase, Walsh transform, Hadamard transform, Haar transform, slant transform Discrete cosine transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms.

UNIT II: IMAGE ENHANCEMENT & IMAGE RESTORATION 9

Introduction to image enhancement, Enhancement in spatial domain, enhancement through point operation, Types of point operation, Histogram manipulation, Linear Gray level transformation, Nonlinear Gray level transformation, Local or neighbourhood operation, Median filter, Image sharpening, Bit plane slicing, Image enhancement in the frequency domain.

Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution

UNIT III: IMAGE SEGMENTATION AND IMAGE COMPRESSION 9

Introduction to image segmentation, Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour

UNIT IV: COLOUR IMAGE PROCESSING

Introduction, Light and colour, colour formation, Human perception of colour, colour model The chromaticity diagram, colour image quantization, Histogram of colour image, colour image filtering, Gamma correction of a colour image, colour image segmentation.

UNIT V: MORPHOLOGICAL IMAGE PROCESSING

Preliminaries-Dilation & Erosion, Opening & Closing, Hit or Miss Transformation, Basic Morphological Algorithms, Extension to Gray scale Images.

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:


1. ATMEL CPLDs – Prochip designer
   a) Schematic entry
   b) VHDL entry
2. AT40K FPGA series – synthesis – design – simulation of application programs
3. Xilinx EDA design tools – device programming –PROM programming
4. ALTERA and Mentor graphics – IC design tools
5. Code compressor studio for embedded DSP using Texas tool kit
6. Cell based ASICs – sample programs for risk and security plans
7. IPCORE usage in VOIP through SoC2 tools
8. FPSLIC synthesis testing and examples
9. Third party tools for embedded java and embedded C++ applications through cadence tools.

TOTAL: 30 HOURS
ELECTIVE

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AIM:

As VLSI implementation is largely in ASIC, this subject is introduced here.

OBJECTIVE:

To make the student learn the fundamentals of ASIC and its design methods.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance - Logical effort –Library cell design - Library architecture

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS PROGRAMMABLE ASIC I/O CELLS

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY


UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL: 45 HOURS

ME EST R 2015
REFERENCES:

AIM:

To understand performance metrics and be able to analyze scalability and speedup factors of multiprocessor systems.

OBJECTIVE:

- To Learn parallel computer architectures with multiprocessor and multi-core.
- To understand Master parallel programming techniques.
- To gain experiences of applying parallel programming to achieve performance gains from multiprocessor and multi-core computer systems.

Unit I
Application-Specific Multiprocessors 9 Hours

Unit II
Dataflow and Scheduling Models 9 Hours

Unit III
Ordered-Transactions Strategy 9 Hours
Shared bus architecture – Inter-processor communication mechanisms - Design of an ordered memory access multiprocessor - Design details of a prototype - Hardware and software implementation - Ordered I/O and parameter control – Inter-processor communication graph (Gipc) - Execution time estimates - Ordering constraints viewed as added edges - Periodicity - Optimal order - Effects of changes in execution times - Effects of inter-processor communication costs - Application examples.

Unit IV
Synchronization 9 Hours

Unit V
Run Time System 9 Hours

REFERENCES:

ME EST R 2015
AIM:

To understand the security principles of wireless networks.

OBJECTIVE:
- To explore variety of attacks and threats and its impact on MAC layer and Network layer
- To study characteristics, vulnerabilities and challenges of ad hoc networks
- To provide solution for covering the security principles and flaws of popular wireless technologies
- To evaluate the performance of secured routing protocols in MANETs.

Unit I – Attacks on Routing Protocols  

Unit II – Intrusion Detection in Wireless Ad Hoc Networks  
Problem in current IDS techniques - requirements of IDS - classification of IDS – Network and host based - anomaly detection, misuse detection, specification based - intrusion detection in MANETs using distributed IDS and mobile agents - AODV protocol based IDS - Intrusion resistant routing algorithms – Comparison of IDS.

Unit III – Mitigating Techniques for Routing Misbehavior  
Watchdog, Parthrater, Packet leashes and RAP.

Unit IV – Secure Routing Protocols:  
Self organized network layer security in MANETs - mechanism to improve authentication and integrity in AODV using hash chain and digital signatures - on demand secure routing protocol resilient to Byzantine failures - ARIADNE, SEAD, SAR, and ARAN.

Unit V – Challenges in Routing Security  
Security - Challenges and solutions - Providing Robust and Ubiquitous security support - Adaptive security for multilevel Ad Hoc Network - Denial of service Attack at the MAC layer - Detection and handling of MAC layer Misbehavior.

REFERENCES:
AIM:
The students can able to analyze the procedure for various principles of Evolutionary computing in real world problem.

OBJECTIVE:
- To study different types of optimization techniques.
- To understand the concepts of genetic algorithms.
- To attain sound knowledge applications of soft computing.

Unit I – Fuzzy Systems 9 Hours

Unit II – Neural Networks 9 Hours

Unit III – Neuro Fuzzy Modeling 9 Hours

Unit IV – Genetic Algorithms 9 Hours

Unit V – Applications of Soft Computing 9 Hours
Fuzzy techniques for inverted pendulum case-SIRM fuzzy systems-MCDM for weather forecasting and financial marketing-Neural networks for pattern recognition-TS problems-Routers - GA application to metabolic modeling.

REFERENCES:
AIM:
To describe and determine the performance of different Image reconstruction techniques.

OBJECTIVE:
- To study about various medical image acquisition methods.
- To understand 2D and 3D image reconstruction techniques.
- To gain sound knowledge about CT, MRI, nuclear and ultrasound imaging.
- To realize the factors those affect the quality of medical images.

Unit I – Acquisition of Images 9 Hours

Unit II – Mathematical Preliminaries for Image Reconstruction 9 Hours

Unit III – Fluoroscopy, CT, Image quality 9 Hours

Unit IV – Magnetic Resonance Imaging and Spectroscopy 9 Hours

Unit V – Ultra sound, Neuro magnetic Imaging 9 Hours

REFERENCES:
AIM:

The students can able to learn advanced technologies in the fields of NOC along with the fundamental concepts.

OBJECTIVE:

- To understand the fundamentals of 3D NOC.
- To impart knowledge about testing and energy issues in NOC.
- To understand the router architectures in 3D NOC.

Unit I
Introduction to Three Dimensional NOC 9 Hours

Unit II
Test and Fault Tolerance of NOC 9 Hours
Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on-Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures- Monitoring Services for Networks-on-Chips.

Unit III
Energy and Power Issues of NOC 9 Hours

Unit IV
Micro-Architecture of NOC Router 9 Hours

Unit V
DimDE Router for 3D NOC 9 Hours
A Novel Dimensionally Decomposed Router for On-Chip Communication in 3D Architectures - Digest of Additional NoC MACROArchitectural Research.

Total: 45 Hours

REFERENCES:
4. Giovanni De Micheli, Luca Benini, Networks on Chips: Technology and Tools (Systems on Silicon), Publisher: Morgan Kaufmann; 1 edition (August 3, 2006).
AIM:

The aim of this course is to develop and deploy advances in measurement science to safely increase the versatility, autonomy, and rapid re-tasking of intelligent robots and automation technologies.

OBJECTIVE:

At the end of this course student will infer some knowledge regarding advanced robotics and automation.

UNIT I INTRODUCTION

Geometric configuration of robots - manipulators - drive systems - internal and external sensors - end effectors - control systems - robot programming languages and applications - Introduction to robotic vision.

UNIT II ROBOT ARM KINEMATICS

Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation - Denavit Hattenberg representation and various arm configurations.

UNIT III ROBOT ARM DYNAMICS


UNIT IV ROBOT APPLICATIONS

Material Transfer & Machine Loading / Unloading General Consideration in robot material handling transfer applications – Machine loading and unloading, Processing Operations Spot welding – Continuous arc welding - spray coating – other processing operations using robots.

UNIT V ASSEMBLY AND INSPECTION

Assembly and robotic assembly automation – Parts presentation methods – assembly operation – Compliance and the Remote Center Compliance(RCC) device – Assembly system Configurations – Adaptable, Programmable assembly system – Designing for robotic assembly – Inspection automation.

TOTAL: 45 HOURS

REFERENCES:

AIM:

The students can able to gain knowledge about SoC Design Methodology.

OBJECTIVE:

- To understand the concepts of System on Chip Design methodology for Logic and Analog Cores.
- To understand the concepts of System on Chip Design Validation.
- To understand the concepts of SOC Testing.

Unit I
Introduction
9 Hours
System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology - SoC design issues -SoC challenges and components.

Unit II
Design Methodological For Logic Cores
9 Hours

Unit III
Design Methodology for Memory and Analog Cores
9 Hours
Embedded memories –Simulation modes Specification of analog circuits – A to D converter –Phase- located loops –High I/O.

Unit IV
Design Validation
9 Hours
Core level validation –Test benches –SoC design validation – Co simulation –hardware/ Software co-verification.
Case Study: Validation and test of systems on chip

Unit V
Soc Testing
9 Hours

Total: 45 Hours

REFERENCES:
AIM:
To gain the knowledge about the procedure for various pattern recognition principles in real world problem.

OBJECTIVE:
➢ To understand different supervised and unsupervised learning techniques.
➢ To obtain sound knowledge on recent advancement on pattern recognition techniques.

Unit I – Pattern Classifier 9 Hours

Unit II – Unsupervised Classification 9 Hours
Clustering for unsupervised learning and classification - Clustering concept - C-means algorithm – Hierarchical clustering procedures - Graph theoretic approach to pattern clustering - Validity of clustering solutions.

Unit III – Structural Pattern Recognition 9 Hours
Elements of formal grammars - String generation as pattern description - Recognition of syntactic description - Parsing - Stochastic grammars and applications - Graph based structural representation.

Unit IV – Feature Extraction and Selection 9 Hours

Unit V – Recent Advances 9 Hours

REFERENCES:

AIM:
To gain the knowledge and skills about various image processing applications.

OBJECTIVE:
- To study the fundamentals of vector and signal spaces.
- To explore the concepts of multi resolution analysis of signals.

**Unit I – Introduction**
9 Hours

**Unit II – Multi Resolution Analysis**
9 Hours
Definition of Multi Resolution Analysis (MRA) – Haar basis - Construction of general orthonormal MRAWavelet basis for MRA – Continuous time MRA interpretation for the DTWT – Discrete time MRABasis functions for the DTWT – PRQMF filter banks.

**Unit III – Continuous Wavelet Transform**
9 Hours
Wavelet Transform - definition and properties - concept of scale and its relation with frequency - Continuous Wavelet Transform (CWT) - Scaling function and wavelet functions (Daubechies, Coiflet, Mexican Hat, Sinc, Gaussian, Bi-Orthogonal) - Tiling of time -scale plane for CWT.

**Unit IV – Discrete Wavelet Transform**
9 Hours

**Unit V – Applications**
9 Hours

**REFERENCES:**
4. www.multiresolution.com
5. www.wavelet.org
AIM:

To apply knowledge from undergraduate engineering and other disciplines to identify, formulate, solve novel advanced electronics engineering along with soft computing and networking problems that require advanced knowledge within the field.

OBJECTIVE:

➢ To study the concepts of biological and artificial neurons
➢ To explore the fundamentals of various algorithms related to supervised neural networks and its applications
➢ To explore the Applications of various algorithms related Genetic algorithms and SVM

Unit I – Fundamental Concepts and Models of Artificial Neural Systems

9 Hours

Biological Neurons and their Artificial models, Models of Artificial Neural Networks, Learning and Adaptation, Neural Network Learning Rules, Single Layer Perceptron Classifiers.

Unit II – BPN and BAM

9 Hours


Unit III – Other Networks

9 Hours


Unit IV – Genetic Algorithms & Implementation Techniques

9 Hours


Unit V – Advances and Applications

9 Hours


REFERENCES:


ME EST R 2015
AIM:

To obtain awareness for adaptation in MAC, IP, protocols for advanced mobile networks.

OBJECTIVE:

➢ To study fundamentals of 4G networks
➢ To explore issues and challenges in designing adaptive MAC for adhoc networks
➢ To understand adaptation of the routing protocols in mobile networks
➢ To explore issues and challenges in sensor network deployment
➢ To develop security protocols for wireless networks

Unit I – Fundamentals of 4G Networks 9 Hours

Unit II – Adaptive MAC and Network Layer 9 Hours

Unit III – Adaptive TCP Layer 9 Hours
Introduction-TCP operations and Performance – TCP for Mobile Cellular Networks-RED Gateways for Congestion Avoidance- TCP for Mobile AdHoc Networks – Cross Layer optimization – Introduction to Mobility Management- Location Registration and Call Delivery in 4G.

Unit IV – AD HOC Networks 9 Hours

Unit V – Sensor Networks and Security 9 Hours

REFERENCES:

AIM:

To become knowledgeable about contemporary developments.

OBJECTIVE:

➢ To study the basics of automotive electronics.
➢ To understand sensors and activators.
➢ To study charging systems.

Unit I – Fundamentals of Automotive Electronics 9 Hours
Current trends in automotive electronic engine management system, electromagnetic interference suppression, electromagnetic compatibility, electronic dashboard instruments, onboard diagnostic system. Security and warning system.

Unit II – Starting System 9 Hours
Condition at starting, behavior of starter during starting, series motor and its characteristics, principle and construction of starter motor, working of different starter drive units, care and maintenances of starter motor. Starter switches.

Unit III – Charging System 9 Hours
Generation of direct current, shunt generator characteristics, armature reaction, third brush regulation, cutout. Voltage and current regulators, compensated voltage regulator, alternators principle and constructional aspects. Bridge rectifiers and new developments.

Unit IV – Batteries and Accessories 9 Hours
Principle and construction of lead acid battery, characteristics of battery, rating capacity and efficiency of batteries, various tests on batteries, maintenance and charging. Lighting system: insulated and earth return system, details of head light and side light, LED lighting system, head light dazzling and preventive methods. Horn, wiper system and trafficator.

Unit V – Sensors and Activators 9 Hours
Types of sensors: sensor for speed, throttle position, exhaust oxygen level, manifold pressure, crankshaft position, coolant temperature, exhaust temperature, air mass flow for engine application. Solenoids. Stepper motors and relay.

REFERENCES:
AIM:
Main aim of this course is to make the students understand in identifying and analyzing the requirements that a distributed multimedia application may enforce on the communication network.

OBJECTIVE:
At the end of this course students have knowledge in distributing multimedia application over the communication network.

UNIT I MULTIMEDIA NETWORKING
Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video.

UNIT II BROAD BAND NETWORK TECHNOLOGY
Broadband services, ATM and IP, IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance.

UNIT III MULTICAST AND TRANSPORT PROTOCOL
Multicast over shared media network, multicast routing and addressing, scaping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP.

UNIT IV MEDIA - ON – DEMAND
Storage and media servers, voice and video over IP, MPEG over ATM/IP, indexing synchronization of requests, recording and remote control.

UNIT V APPLICATIONS
MIME, Peer-to-peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy.

TOTAL HOURS: 45

REFERENCES:
AIM:

The aim of the course is to teach students to use digital signal processors such as the TMS320C6xxx to perform real-time DSP on real signals.

OBJECTIVE:

This course brings together some of the theory and understanding you have gained in several other lecture courses and lets you apply that theory in solving the type of problem which might be encountered by a DSP engineer in industry.

UNIT I: FUNDAMENTALS OF PROGRAMMABLE DSP'S


UNIT II: TMS320C5X PROCESSOR

Architecture – Assembly Language syntax- Addressing modes- Assembly language Instructions – pipeline structure, Operation – Block diagram of DSP Starter kit – Application Programs for processing real time signals.

UNIT III: TMS320C3X PROCESSOR

Architecture – Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation – Block diagram of DSP starter kit – Application, Programs for processing real time systems – Generating and finding the sum of series, Convolution of two sequences , Filter design.

UNIT IV: ADSP PROCESSORS

Architecture of ADSP-21XX and ADSP – 210XX series of DSP processors – Addressing modes and Assembly language instructions – Applications programs – Filter design, FFT calculation- Blackfin DSP Processor

UNIT V: ADVANCED PROCESSORS


TOTAL: 45 HOURS

TEXT BOOK:


REFERENCES:

1. User guides Texas Instrumentation, Analog Devices, Motorola.
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**AIM:**

Since the concepts of real time systems and their analysis is very essential for embedded students this subject is given.

**OBJECTIVE:**

To make the student learn, all real time aspects of various system components, like OS, memory, communication and an introduction to reliability evaluation methods.

**UNIT I INTRODUCTION**

Introduction - issues in real time computing - structure of a real time system - task classes - performance measures for real time systems - estimating program run times - task assignment and scheduling - classical uniprocessor scheduling algorithms - uniprocessor scheduling of IRIS tasks - tasks assignment - mode changes - fault tolerant scheduling.

**UNIT II PROGRAMMING LANGUAGES AND TOOLS**

Language features - desired language characteristics - data typing - control structures - facilitating hierarchical decomposition - package - run-time error handling - overloading and generics - multitasking - low level programming - task scheduling - timing specifications - programming environments - run-time support – code generation.

**UNIT III REAL TIME DATABASES**

Real time database - basic definition - real time Vs general-purpose database - main memory databases - transaction priorities - transaction aborts - concurrency control issues - disk scheduling algorithms - two-phase approach to improve predictability - maintaining serialization consistency - databases for hard real time systems.

**UNIT IV COMMUNICATION**


**UNIT V EVALUATION TECHNIQUES**

Reliability evaluation techniques - reliability models for hardware redundancy - software error models – response time calculation – interrupt latency – time loading and its measurement – reducing response times – analysis of memory requirements – reducing memory loading

**TOTAL: 45 HOURS**

ME EST R 2015
TEXT BOOK:

REFERENCES:
AIM:

To expose students to the advanced digital signal processing systems for VLSI and associated EDA Tools.

OBJECTIVE:

At the end of this course the student will be able knowing methods and techniques for implementation of DSP systems.

UNIT I    INTRODUCTION TO DSP SYSTEMS
Introduction To DSP Systems - Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II    RETIMING
Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT III    FAST CONVOLUTION

UNIT IV    BIT-LEVEL ARITHMETIC ARCHITECTURES
Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement.

UNIT V    PROGRAMMING DIGITAL SIGNAL PROCESSORS
Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low
power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

TOTAL: 45 HOURS

REFERENCES:
AIM:

As there is always a need for power efficient circuits and devices, this course explains the methods for low power VLSI design.

OBJECTIVE:

At the end of this course the student will be able to design Low power CMOS designs, for digital circuits.

UNIT I

SIMULATION & PROBABILISTIC POWER ANALYSIS

Introduction - Simulation - Power Analysis-Probabilistic Power Analysis.

UNIT II

CIRCUIT, LOGIC & SPECIAL TECHNIQUES


UNIT III

ADVANCED TECHNIQUES & PHYSICS OF POWER DISSIPATION


UNIT IV

POWER ESTIMATION & SYNTHESIS FOR LOW POWER


UNIT V

STATIC RAM & SOFTWARE DESIGN FOR LOW POWER


TOTAL: 45 HOURS

REFERENCES:

AIM:
The aim of this course is provide an introduction of an advanced element of learning in the field of wireless communication and also expose the students to the concepts of wireless devices and mobile computing.

OBJECTIVE:
At the end of this course the student should be able to understand the concept of mobile computing and architecture of mobile communication.

UNIT I INTRODUCTION
9
Basics of mobile computing - Medium access control – Telecommunication systems – Satellite systems – Broadcast systems.

UNIT II STANDARDS
9
Wireless LAN – IEEE 802.11 – Frequency Hopping spread spectrum – Direct sequence and spread spectrum - HIPERLAN – Bluetooth.

UNIT III ADHOC NETWORKS
9

UNIT IV NETWORK ISSUES
9

UNIT V APPLICATION ISSUES
9

TOTAL: 45 HOURS

REFERENCES:

ME EST R 2015


AIM:
To use modern engineering tools, software and equipments to analyze problems.

OBJECTIVE:
- To learn the fundamental principles of feedback control and dynamic systems
- To acquire the concepts of Optimal Control Systems and Digital Control Systems
- To Model and control hybrid systems
- To learn how to perform the stability analysis of Feedback Control Systems

Unit I
Introduction to Control Systems 9 Hours
Brief History of Automatic Control - Engineering Design - Control System Design - Differential Equations of Physical Systems - Linear Approximations of Physical Systems - The Transfer Function of Linear Systems - The State Variables of a Dynamic System - The State Differential Equation - The Transfer Function from the State Equation - The Time Response and the State Transition Matrix

Unit II
Feedback Control System 9 Hours

Unit III
The Stability of Linear Feedback Systems 9 Hours

Unit IV
Frequency Response 9 Hours

Unit V
Sampled-Data Systems 9 Hours

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES: