VINAYAKA MISSIONS UNIVERSITY, SALEM
TAMILNADU, INDIA.

FACULTY OF ENGINEERING & TECHNOLOGY

SCHOOL OF ELECTRONIC SCIENCES

M.E.- VLSI DESIGN

PART TIME

AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY, PAIYANOOR

&

V.M.K.V. ENGINEERING COLLEGE, SALEM

CHOICE BASED CREDIT SYSTEM

2012 REGULATION
## I SEMESTER

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AIM:

Mathematics is fundamental for any field of technology. The aim of the subject is to impart essential mathematical topics for the PG courses in Electronics and Communication Engineering Department.

OBJECTIVE:

To make the student learn to apply mathematics in their field with the advanced topics as fuzzy logic, dynamic programming etc...

UNIT I: FUZZY LOGIC

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II: MATRIX THEORY


UNIT III: ONE DIMENSIONAL RANDOM VARIABLES

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform,

Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV: DYNAMIC PROGRAMMING


UNIT V: QUEUEING MODELS


TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

REFERENCES:

AIM:

Learning design of digital circuits is a fundamental necessity for designing embedded systems. This subject provides necessary instruments to achieve that goal.

OBJECTIVE:

To make the student learn: theory of logic and logic functions, design of digital circuits, and an introduction to VHDL language.

UNIT I: ADVANCED TOPICS IN BOOLEAN ALGEBRA 9
Shannon's expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT / INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

UNIT II: THRESHOLD LOGIC 9
Linear separability, Unateness, Physical implementation, Dual comparability, reduced functions, various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

UNIT III: SYMMETRIC FUNCTIONS 9
Elementary symmetric functions, partially symmetric and totally symmetric functions, Mc Cluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

UNIT IV: SEQUENTIAL LOGIC CIRCUITS 9
Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

UNIT V: PROGRAMMABLE LOGIC DEVICES 9
Basic concepts, Programming technologies, Programmable Logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Structure of Standard PLD's, Complex PLD's (CPLD). System Design Using PLD's - Design of combinational and sequential circuits using PLD's, Programming PAL device using PALASM, Design of state machine using Algorithmic State Machines (ASM) chart as a design tool. Introduction To Field Programmable Gate Arrays - Types of FPGA, Xilinx XC3000 series, Logic Cell array (LCA), Configurable Logic Blocks (CLB) Input/Output Block (IOB)- Programmable Interconnect Point (PIP), Introduction to Actel ACT2 family and Xilinx XC4000 families, Design examples.

TOTAL: 45 HOURS

REFERENCES:
AIM:

- The aim of this course is to describe the design, technology and manufacture of MOS integrated circuits and future nanoscale electron devices.
- It will provide a firm foundation for those wishing to pursue careers in applications or in research/development in the field of semiconductor devices/circuits.

OBJECTIVES:

On completion of the module students should have developed an awareness of the requirements for IC technology. Understand how device miniaturization has led to improved device performance and the potential limits to this process.

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II INVERTERS AND LOGIC GATES. 9

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL 9

PHYSICAL DESIGN.


UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE 9

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS
TEXT BOOK:

REFERENCES
AIM:
As VLSI implementation is largely in ASIC, this subject is introduced here.

OBJECTIVE:
To make the student learn the fundamentals of ASIC and its design methods.

UNIT I  INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II  PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMABLE ASIC I/O CELLS

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III  PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY


UNIT IV  LOGIC SYNTHESIS, SIMULATION AND TESTING

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation, Introduction to JTAG.

UNIT V  ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL: 45 HOURS
REFERENCES:

AIM:

This course deals with fundamentals of electronics involved in the design of VLSI circuits.

OBJECTIVES:

At the end of the course, students should be able to understand

- CMOS processing technology and Basic CMOS circuits, characteristics and performance.
- Designing of combinational and sequential circuits in CMOS.

UNIT I: MOSFET DEVICE PHYSICS

MOSFET capacitor, Basic operation, Basic modeling, Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and A.C small signal modeling, model parameter extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II: NOISE MODELING

Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, model for accurate distortion analysis, nonlinearities in CMOS devices and modeling, calculation of distortion in analog CMOS circuits

UNIT III: BSIMV4 MOSFET MODELING

Gate dielectric model, Enhanced model for effective DC and AC channel length and width, Threshold voltage model, Channel charge model, mobility model, Source/drain resistance model, I-V model, gate tunneling current model, substrate current models, Capacitance models, High speed model, RF model, noise model, junction diode models, Layout-dependent parasitics model.

UNIT IV: OTHER MOSFET MODELS

The EKV model, model features, long channel drain current model, modeling second order effects of the drain current, modeling of charge storage effects, Non-quasi-static modeling, noise model temperature effects, MOS model 9, MOSAI model)
UNIT V: MODELLING OF PROCESS VARIATION AND QUALITY ASSURANCE

Influence of process variation, modeling of device mismatch for Analog/RF Applications, Benchmark circuits for quality assurance, Automation of the tests

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:

LIST OF EXPERIMENTS

1. Design Entry Using VHDL or Verilog examples for circuit descriptions using HDL languages sequential and concurrent statements.
2. Structural and behavioral descriptions, principles of operation and limitation of HDL simulators. Examples of sequential and combinational logic design and simulation. Test vector generation.
4. FPGA programming, I/O interfacing, Analog interfacing, Real time application development.
5. SPICE simulations for small size standard cells.

TOTAL: 30 HOURS

REFERENCES:

AIM:

The key aim of this module is to provide the background and the methods for the understanding of the operation of basic analogue CMOS cells, and how to design common functions.

OBJECTIVE:

After this course the students can adopt strongly industrial perspective and design methods for manufacturability and robustness as well as cost are given high priority.

UNIT I: MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES


UNIT II: CIRCUIT CONFIGURATION FOR LINEAR IC


UNIT III: OPERATIONAL AMPLIFIERS

Applications of operational amplifiers, Deviations from ideality in real operational amplifiers, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise.

UNIT IV: ANALOG MULTIPLIER AND PLL

Precision Rectification- Analog Multipliers employing the bipolar transistor, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits, Noise in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature.

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Basic Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers.

TOTAL: 45 HOURS

TEXT BOOK:


REFERENCE BOOKS:

1. Behzad Razavi, “Principles of data conversion system design”, S.Chand and company Ltd, 2000
AIM:
The aim of this course is to give the students knowledge about the usage of computer for the design of VLSI circuits. It also provides the flow of process involved and how design can be simulated.

OBJECTIVE:
At the end of this course the student will have knowledge in using computer simulation software for designing the VLSI circuits.

UNIT I

UNIT II
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III
Floorplanning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV
Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V
High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:
AIM:
Any VLSI design mostly involves processor systems, this course describes computer architectures.

OBJECTIVES:
- At the end of this course the student will know various parallel processing applications and their performance towards real time computing.
- To impart knowledge on scalable architectures and the performances.

UNIT I- THEORY OF PARALLELISM, PARTITIONING AND SCHEDULING  9
Parallel Computer models: The state of computing, Multiprocessors and Multicomputers, Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks.
Program and network properties: Conditions of parallelism, Program partitioning and scheduling, program flow mechanisms, System interconnect architectures.

UNIT II- SCALABLE PERFORMANCES & HARDWARE TECHNOLOGIES  9
Principles of scalable performance: Performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.
Processor and memory hierarchy: Advanced processor technology, Superscalar and vector processors, memory hierarchy technology, virtual memory technology.

UNIT III- MEMORY ORGANIZATIONS & PIPELINING  9
Bus cache and shared memory: backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.
Pipelining: Linear and non-Linear Pipeline processors-Instruction pipeline design and Arithmetic pipeline design.

UNIT IV- PARALLEL & SCALABLE ARCHITECTURES  9
Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V- SOFTWARE & PARALLEL PROCESSING  9
Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL: 45 HOURS

TEXT BOOKS:

REFERENCE BOOKS:
### AIM:
This subject provides all basic concepts of embedded systems and their implementation in C language.

### OBJECTIVE:
To make the student learn, the embedded system implementation in C language.

### UNIT I INTRODUCTION
Examples of Embedded Systems, Typical hardware, Terminology, Gates, Timing diagrams, Memory, Microprocessors, buses, direct memory access, interrupts, built-ins on the microprocessor, conventions used on schematics.

### UNIT II INTERRUPTS & SOFTWARE ARCHITECTURES
Interrupt basics, shared data problem, interrupt latency; Software architectures – Round Robin, Round Robin with interrupts, function queue scheduling architecture, real time operating system architecture, selecting an architecture.

### UNIT III - INTRODUCTION TO REAL TIME OPERATING SYSTEMS AND OPERATING SYSTEM SERVICES
Tasks and task states, Tasks and data, semaphores and shared data, Message queues, Mailboxes and pipes, Timer functions, Events, Memory management, Interrupt routines in an RTOS environment.

### UNIT IV EMBEDDED SOFTWARE DEVELOPMENT AND DEBUGGING TECHNIQUES
The compilation process, native versus cross compilers, Libraries – run time libraries, writing a library, using alternative libraries, using a standard library, Porting kernels, Downloading. Debugging techniques, Emulation techniques.

### UNIT V BASIC DESIGN USING A REAL TIME OPERATING SYSTEM & DESIGN EXAMPLES
Principles, Encapsulating semaphores and queues, Hard time scheduling considerations, saving memory space and power.

Embedded system design and coding for an automatic chocolate vending machine, case study of an embedded system for an adaptive cruise control system in a car, case study of an embedded system for a smart card.

**TOTAL: 45 HOURS**

### TEXT BOOKS:

### REFERENCE BOOKS:
1.) Implementation of 8 Bit ALU in FPGA / CPLD.
2.) Implementation of 4 Bit Sliced processor in FPGA / CPLD.
3.) Implementation of Elevator controller using embedded microcontroller.
4.) Implementation of Alarm clock controller using embedded microcontroller.
5.) Implementation of model train controller using embedded microcontroller.
6.) System design using PLL.
AIM:

To enhance the knowledge of student with various algorithms and techniques to apply in controllers.

OBJECTIVE:
- To study the basic digital control system design and its stability testing.
- To study the models of digital devices and systems.
- To learn about digital control algorithms.
- To study about control systems analysis using state variable methods.
- To analyse the control systems using state variable methods.

Unit I Digital Control, Signal Processing in digital control


Unit II Models of Digital Control Devices and Systems


Unit III Design of digital Control Algorithms


Unit IV Control System analysis using state Variable Methods


Unit V Practical Aspects of Digital Control Algorithms
Mechanisation of control Algorithms using Microprocessors – Microprocessor Based Temperature Control Systems–Case Study – Stepping Motors and their Interfacing to Microprocessors

**TOTAL HOURS: 45**

**Text Books**


**Reference Books:**

**ELECTIVE**

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<td>LOW POWER VLSI DESIGN</td>
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**AIM:**

As there is always a need for power efficient circuits and devices, this course explain the methods for low power VLSI design.

**OBJECTIVE:**

At the end of this course the student will be able to design Low power CMOS designs, for digital circuits.

**UNIT I**

Introduction - Simulation - Power Analysis-Probabilistic Power Analysis.

**UNIT II**


**UNIT III**


**UNIT IV**


**UNIT V**


**TOTAL HOURS: 45**

**REFERENCES:**

AIM:

To expose students to the advanced digital signal processing systems for VLSI and associated EDA Tools.

OBJECTIVE:

At the end of this course the student will be able knowing methods and techniques for implementation of DSP systems.

UNIT I  INTRODUCTION TO DSP SYSTEMS 9
Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II  RETIMING 9
Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT III  FAST CONVOLUTION 9

UNIT IV  BIT-LEVEL ARITHMETIC ARCHITECTURES 9
Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement.

UNIT V  PROGRAMMING DIGITAL SIGNAL PROCESSORS 9
Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low
power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS
leakage current, basic principles of low power design.

TOTAL HOURS: 45

REFERENCES:
3. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill,
1994.
1985.
5. Jose E. France, Yannis Tsividis, "Design of Analog - Digital VLSI Circuits for Telecommunication
AIM:
Analog circuits are essential in interfacing and in building amplifiers and low pass filters. This course introduces design methods for CMOS analog circuit design and implementation of standard MOS integrated circuits and be able to assess their performance taking into account the effects of real circuit parameters.

OBJECTIVE:
At the end of this course the student will be learning, CMOS analog circuits design and simulation using SPICE.

UNIT I - MOS TRANSISTOR THEORY

UNIT II - CMOS PROCESSING TECHNOLOGY

UNIT II - CIRCUIT CHARACTERISTICS AND PERFORMANCE ESTIMATION

UNIT IV - CMOS CIRCUIT AND LOGIC DESIGN

UNIT V - CMOS SUBSYSTEM DESIGN

REFERENCES


Total Hours: 45
AIM:
This course is intended to introduce the student to learn about Device Modeling- Various types of analog systems- CMOS amplifiers and Comparators.

OBJECTIVE:
By the end of the term, students should be able to:

- Demonstrate an understanding of MOS terminal characteristics and capacitive effects.
- Create integrated circuit layouts showing an awareness of the underlying process technology and layout parasitic as well as their impact on circuit performance.

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT-MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING
Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks -Floating-Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS
UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT

9


TOTAL: 45 HOURS

REFERENCES:
**AIM:**

Testing VLSI is essential as these circuits are complex. Hence this paper deals with fundamental techniques used for logic testing.

**OBJECTIVE:**

At the end of the course the student will be having knowledge on digital testing as applied to VLSI design.

**UNIT I BASICS OF TESTING AND FAULT MODELLING**

**UNIT II TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS**
Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

**UNIT III DESIGN FOR TESTABILITY**
Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

**UNIT IV SELF – TEST AND TEST ALGORITHMS**

**UNIT V FAULT DIAGNOSIS**
Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

**Total Hours: 45**

**REFERENCES:**
AIM:
This course will introduce approaches and methodologies for VLSI architectures of signal processing.

OBJECTIVE:
- At the end of this course the student can have knowledge about the basic approaches and methodologies for VLSI architectures of signal processing.
- The students will also have hands-on VLSI system design experience using hardware description language (HDL) and commercial EDA tools (Synopsys).

1. INTRODUCTION
Overview of digital VLSI design methodologies - Trends in IC technology – advanced Boolean algebra - Shannon’s expansion theorem - consensus theorem - Octal designation - Run measure - Buffer gates - Gate Expander - Reed Muller expansion - Synthesis of multiple output combinational logic circuits by product map method - Design of static hazard free and dynamic hazard free logic circuits.

2. ANALOG VLSI AND HIGH SPEED VLSI
Introduction to analog VLSI - Realisation of Neural networks and switched capacitor filters - sub-micron technology and GaAs VLSI technology.

3. PROGRAMMABLE ASICS
Anti fuse – static RAM – EPROM and EEPROM technology - PREP bench marks –Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC & AC inputs and outputs-clock and power inputs - Xilinx I/O blocks.

4. PROGRAMMABLE ASIC DESIGN SOFTWARE

5. LOGIC SYNTHESIS, SIMULATION AND TESTING
Basic features of VHDL language for behavioural modelling and simulation - Summary of VHDL data types – dataflow and structural modelling – VHDL and logic synthesis – types of simulation – boundary scan test-fault simulation – automatic test pattern generation

TOTAL HOURS: 45
REFERENCES:
2. Amar Mukherjee, Introduction to NMOS and CMOS VLSI system design, Prentice hall 1986
4. Frederick J. Hill and Gerald R. Peterson, “Computer Aided Logical Design with emphasis on VLSI”.
AIM:
This course aims to provide students with an understanding of digital image processing techniques, including image reconstruction and restoration, segmentation and enhancement, also colour and morphological image processing techniques.

OBJECTIVE:
Upon successful completion of this course, students should be able to understand all types of image processing techniques.

UNIT I: INTRODUCTION TO IMAGE PROCESSING SYSTEMS & IMAGE TRANSFORMS 9

Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Applications of Digital image processing

Introduction, Need for transform, Image transforms, Fourier transform, 2 D Discrete Fourier transform and its transforms, Importance of phase, Walsh transform, Hadamard transform, Haar transform, slant transform, Discrete cosine transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms.

UNIT II: IMAGE ENHANCEMENT & IMAGE RESTORATION 9

Introduction to image enhancement, Enhancement in spatial domain, enhancement through point operation, Types of point operation, Histogram manipulation, Linear Gray level transformation, Nonlinear Gray level transformation, Local or neighbourhood operation, Median filter, Image sharpening, Bit plane slicing, Image enhancement in the frequency domain.

Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution

UNIT III: IMAGE SEGMENTATION AND IMAGE COMPRESSION 9

Introduction to image segmentation, Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour

Introduction, Need for image compression, Redundancy in images, Classification of redundancy in images, image compression scheme, Classification of image compression schemes, Fundamentals of information theory, Run length coding, Shannon – Fano coding, Huffman coding, Arithmetic coding,
Predictive coding, Transformed based compression, Image compression standard, Wavelet-based image compression

UNIT IV: COLOUR IMAGE PROCESSING

Introduction, Light and colour, colour formation, Human perception of colour, colour model The chromaticity diagram, colour image quantization, Histogram of colour image, colour image filtering, Gamma correction of a colour image, colour image segmentation.

UNIT V: MORPHOLOGICAL IMAGE PROCESSING

Preliminaries-Dilation & Erosion, Opening & Closing, Hit or Miss Transformation, Basic Morphological Algorithms, Extension to Gray scale Images.

TOTAL: 45 HOURS

REFERENCE BOOKS:


AIM:
This course aims to provide the student to apply engineering knowledge and specialist techniques to prevent or to reduce the likelihood or frequency of failures.

OBJECTIVE:
The students will be able to understand the ways in which product fail, the effects of failure and aspects of design, manufacture, maintenance and use which affect the likelihood of failure.

UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE
9
Statistical distribution, statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference, Safety margin and loading roughness on reliability.

UNIT II RELIABILITY PREDICTION, MODELLING AND DESIGN
9
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY
9
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design, software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS
9
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MANAGEMENT
9
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

TOTAL HOURS: 45

REFERENCES:
AIM:

To understand different electromagnetic Interference problems occurring in Intersystem and in inter system and their possible mitigation techniques in Electronic design.

OBJECTIVES:

➢ To understand EMI Sources, EMI problems and their solution methods in PCB level / Subsystem and system level design.

➢ To measure the emission immunity level from different systems to couple with the prescribed EMC standards.

UNIT I EMI/EMC CONCEPTS

EMI- EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBS

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL HOURS: 45

REFERENCES:

AIM:
Students will be introduced to actual advanced issues related to signal processing, mainly using time-frequency signal analysis.

OBJECTIVE:
The goal of advanced digital signal processing course is to provide a comprehensive coverage of signal processing methods and tools, including leading algorithms for various applications.

1. DISCRETE RANDOM SIGNAL PROCESSING

2. SPECTRUM ESTIMATION

3. LINEAR ESTIMATION AND PREDICTION

4. ADAPTIVE FILTERS

5. MULTIRATE DIGITAL SIGNAL PROCESSING
Mathematical description of change of sampling rate - Interpolation and Decimation - continuous time model - Direct digital domain approach - Decimation by an integer factor - Interpolation by an integer factor - Single and multistage realization - poly phase realization - Application to sub band coding - Wavelet transform and filter bank implementation of wavelet expansion of signals.
TOTAL: 45 HOURS

Text Books:

References:
AIM:

The use of real time operating systems has become a necessity to build complex embedded systems, this subject is provided.

OBJECTIVE:

To make the student learn fundamentals of Operating Systems, implementation aspects of real time concepts and few applications on RTOS.

UNIT I: REVIEW OF OPERATING SYSTEMS


UNIT II: OVERVIEW OF RTOS

RTOS Task and Task state - Process Synchronisation- Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronisation problem – Deadlocks -

UNIT I II: REAL TIME MODELS AND LANGUAGES

Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT I V: REAL TIME KERNEL


UNIT V: RTOS APPLICATION DOMAINS


TOTAL HOURS: 45

REFERENCES:


AIM:
To make the student learn: use of C language for embedded applications, real time UML concepts, co-design methods.

OBJECTIVE:
- To study basic programming concepts
- To learn the C and assembly.
- To learn about object oriented analysis and design.
- To learn about UML and its architectures.

1. LOW LEVEL PROGRAMMING IN C

2. C AND ASSEMBLY

3. OBJECT-ORIENTED ANALYSIS AND DESIGN

4. UNIFIED MODELLING LANGUAGE

5. CASE STUDIES

TOTAL HOURS: 45

REFERENCES:
2. Hassan Gomma, “Designing Concurrent, Distributed, and Real-Time applications with UML.”
AIM:
This course is an introduction to MEMS, which also uses micro electronics. This course fulfills the need of electronic engineer who want to create MEMS devices.

OBJECTIVE:
At the end of this course, the student will have knowledge on MEMS materials, fabrication and micro sensor design.

UNIT I MEMS AND MICROSYSTEMS
Typical MEMs and Microsystems, materials for MEMS - active substrate materials- Silicon and its compounds, Silicon piezoresistors, Gallium Arsenide, quartz, polymers. Micromachining-photolithography, thin film deposition, doping, etching, bulk machining, wafer bonding, LIGA

UNIT II MICROSENSORS AND ACTUATORS
Mechanical sensors and actuators – beam and cantilever, piezoelectric materials, thermal sensors and actuators- micromachined thermocouple probe, Peltier effect heat pumps, thermal flow sensors, Magnetic sensors and actuators- Magnetic Materials for MEMS, Devices

UNIT III MICRO OPTO ELECTRO MECHANICAL SYSTEMS
Fundamental principle of MOEMS technology, light modulators, beam splitter, microlens, digital micromirror devices, light detectors, optical switch

UNIT IV MICROFLUIDIC SYSTEMS
Microscale fluid, expression for liquid flow in a channel, fluid actuation methods, dielectrophoresis, microfluid dispensor, microneedle, micropumps-continuous flow system

UNIT V APPLICATIONS OF MEMS
Drug delivery, micro total analysis systems (MicroTAS) detection and measurement methods, microsystem approaches to polymerase chain reaction (PCR), DNA hybridization, Electronic nose, Bio chip

TOTAL HOURS: 45

REFERENCE BOOK:

### AIM:

The aim of this course is to provide an introduction to the advanced element of learning in the field of wireless communication and to expose students to the concepts of wireless devices and mobile computing.

### OBJECTIVE:

At the end of this course, the student should be able to understand the concept of mobile computing and the architecture of mobile communication.

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<th>UNIT – II: TELECOMMUNICATION SYSTEM</th>
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<th>UNIT – III: WIRELESS LAN</th>
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<th>UNIT – IV: MOBILE NETWORK LAYER</th>
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<td>Mobile IP- Dynamic post configuration protocol- mobile Adhoc network- DSDV- DSR- AODV- ZRP- OVMR.</td>
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<th>UNIT – V: MOBILE TRANSPORT LAYER AND APPLICATION</th>
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<td>TCP- WAP- Architecture- WDGP- WTLS- WTP- WSP- WML- WAE- WML script- WTA.</td>
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**TOTAL HOURS: 45**

**TEXT BOOK**


**REFERENCE**

AIM:
To learn all parts of communication software in layered architecture.

OBJECTIVE:
- To study the basics on computer networks and its protocols
- To study the transport layer protocol of OSI model.
- To learn about network layer of OSI model.
- To study data link and MAC layer of OSI model.
- To learn about network security in computer networks.

UNIT I OVERVIEW OF COMPUTER NETWORKS AND APPLICATION LAYER PROTOCOLS
An introduction to internet - An overview of circuit switching - Packet switching and message switching - Routing in data networks - Access networks and physical media - Protocol; layers - Comparison of OSI and Internet protocol stack - Internet backbones - Network access points and ISPS, Application layer protocols - Service provided by the Internet transport protocols – Network applications: www - Overview of HTTP - HTTP message format - User server interaction – Web caches FTP - FTP commands and replies - Electronic mail in the internet - SMPT, MIME – Mail access protocols - POP3 DNS - Introduction to socket programming with TCP and UDP.

UNIT II TRANSPORT LAYER PROTOCOLS
Transport layer services and principles - Relationship between transport and network layers - Overview of transport layer in the internet - Multiplexing and demultiplexing applications connectionless and connection oriented transports - Principles of reliable data transfer – Principles of congestion control.

UNIT III NETWORK LAYER

UNIT IV DATA LINK AND MAC LAYER
Data link layer services and adapters - Error detection and correction techniques – Multiple Access protocols and LANs - LAN addresses and ARP - Ethernet - Hubs - Bridges and Switches PPP- ATM- X.2.5 and Frame relay.

UNIT V NETWORK SECURITY AND MULTIMEDIA
Networks security - Principles of cryptography - Authentication - Integrity - Key distribution and certification - Secure Email - Internet commerce - Network layer security - Multimedia networking application - Streaming stored audio and video - Internet phone - Case study - RTP.

REFERENCE BOOKS:

TOTAL HOURS: 45
ELECTIVE

DSP PROCESSORS

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AIM:

The aim of the course is to teach students to use digital signal processors such as the TMS320C6xxx to perform real-time DSP on real signals.

OBJECTIVE:

This course brings together some of the theory and understanding you have gained in several other lecture courses and lets you apply that theory in solving the type of problem which might be encountered by a DSP engineer in industry.

UNIT I: FUNDAMENTALS OF PROGRAMMABLE DSP’S


UNIT II: TMS320C5X PROCESSOR

Architecture – Assembly Language syntax- Addressing modes- Assembly language Instructions – pipeline structure, Operation – Block diagram of DSP Starter kit – Application Programs for processing real time signals.

UNIT III: TMS320C3X PROCESSOR

Architecture –Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation – Block diagram of DSP starter kit – Application, Programs for processing real time systems – Generating and finding the sum of series, Convolution of two sequences, Filter design.

UNIT IV: ADSP PROCESSORS

Architecture of ADSP-21XX and ADSP – 210XX series of DSP processors – Addressing modes and Assembly language instructions – Applications programs – Filter design, FFT calculation- Blackfin DSP Processor

UNIT V: ADVANCED PROCESSORS


TOTAL: 45 HOURS

TEXT BOOK:

REFERENCE BOOKS:
1. User guides Texas Instrumentation, Analog Devices, Motorola.
AIM:

This course will provide a comprehensive and structured exposure to Soft Computing Techniques i.e Artificial Neural Networks, Fuzzy Logic, Genetic Algorithm, Particle Swarm Optimization.

OBJECTIVE:

To make the student learn, all types of soft computing techniques and how it is applied in various fields.

1. INTRODUCTION

2. ARTIFICIAL NEURAL NETWORKS
Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron. Learning and Training the neural network. Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations. Hopfield network, Self-organizing network and Recurrent network. Neural Network based controller

3. FUZZY LOGIC SYSTEM
Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning. Introduction to fuzzy logic modeling and control. Fuzzification, inferencing and defuzzification. Fuzzy knowledge and rule bases. Fuzzy modeling and control schemes for nonlinear systems. Self-organizing fuzzy logic control. Fuzzy logic control for nonlinear time-delay system.

4. GENETIC ALGORITHM
Basic concept of Genetic algorithm and detail algorithmic steps, adjustment of free parameters. Solution of typical control problems using genetic algorithm. Concept on some other search techniques like tabu search and ant-colony search techniques for solving optimization problems.

5. APPLICATIONS
REFERENCES:
AIM:
The aim of this course is to develop and deploy advances in measurement science to safely increase the versatility, autonomy, and rapid re-tasking of intelligent robots and automation technologies.

OBJECTIVE:
At the end of this course student will infer some knowledge regarding advanced robotics and automation.

UNIT I INTRODUCTION
Geometric configuration of robots - manipulators - drive systems - internal and external sensors - end effectors - control systems - robot programming languages and applications - Introduction to robotic vision.

UNIT II ROBOT ARM KINEMATICS
Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation - Denavit Hattenberg representation and various arm configurations.

UNIT III ROBOT ARM DYNAMICS

UNIT IV ROBOT APPLICATIONS

UNIT V ASSEMBLY AND INSPECTION
Assembly and robotic assembly automation – Parts presentation methods – assembly operation – Compliance and the Remote Center Compliance(RCC) device – Assembly system Configurations – Adaptable, Programmable assembly system – Designing for robotic assembly – Inspection automation.

REFERENCES:
**AIM:**
To provide in depth knowledge to students about the artificial neural networks and also Fuzzy Logic as well as application of it.

**OBJECTIVE:**
- To make the student learn to improve their skills over artificial neural network and their application.
- To make the student learn to understand the concepts of fuzzy logic and their application.

**UNIT I FUNDAMENTALS OF ANN**

**UNIT II ANN ALGORITHM**

**UNIT III APPLICATION OF ANN**

**UNIT IV INTRODUCTION TO FUZZY LOGIC**

**UNIT V APPLICATION OF FUZZY LOGIC**

**TOTAL HOURS: 45**

**REFERENCE BOOKS:**
AIM
The purpose of Video Processing course is to cover the fundamentals of digital video signal
generation and further processing over the communication systems.

OBJECTIVE
To learn the basic concepts of video processing
To learn about the various methodologies for motion estimation
To learn the basic concepts of coding systems
To understand about the waveform based video coding techniques
To understand about the content dependent and scalable video coding techniques

UNIT I VIDEO FORMATION, PERCEPTION AND REPRESENTATION  9

UNIT II TWO-DIMENSIONAL MOTION ESTIMATION    9
General Methodologies, Pixel-Based Motion Estimation,, Block Matching Algorithm, Mesh-based Motion estimation, Global Motion Estimation, Region –Based Motion Estimation, Mutiresolution Motion Estimation, Application of Motion Estimation in Video Coding. Feature-based Motion Estimation.

UNIT III FOUNDATONS OF VIDEO CODING      9
Overview of Coding Systems, Basic Notions in Probability and Information Theory, Information Theory for Source Coding, Binary Encoding, Scalar Quantization , Vector Quantization.

UNIT IV WAVEFORM-BASED VIDEO CODING     9
Block-Based Transform Coding, Predictive Coding, Video Coding Using Temporal Prediction and Transform Coding.

UNIT V CONTENT-DEPENDENT & SCALABLE VIDEO CODING   9
Two-Dimensional Shape Coding, Texture coding for Arbitrarily Shaped Regions, Joint Shape & Texture Coding, Region-Based Video Coding, Object-based Video Coding. Basic Modes of Scalability, Object Based Scalability, Wavelet-transform Based Coding.

TOTAL HOURS: 45

TEXT BOOKS:

REFERENCES:
ELECTIVE | L | T | P | C
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CYBER SECURITY | 3 | 0 | 0 | 3

AIM
To produce the knowledge on cyber security essentials

OBJECTIVE
- To study the cyber security fundamentals
- To study the various techniques on attack and exploitation
- To study in detail about malicious code
- To study about defense and analysis techniques

UNIT I CYBER SECURITY FUNDAMENTALS

UNIT II ATTACKER TECHNIQUES AND MOTIVATIONS
Antiforensics – Tunneling techniques – Fraud Techniques - Threat Infrastructure.

UNIT III EXPLOITATION
Techniques to gain a foot hold – Misdirection, Reconnaissance, and disruption methods.

UNIT IV MALICIOUS CODE

UNIT V DEFENSE AND ANALYSIS TECHNIQUES

TOTAL HOURS: 45

TEXT BOOK

REFERENCE BOOKS