VINAYAKA MISSIONS UNIVERSITY, SALEM
TAMILNADU, INDIA.

FACULTY OF ENGINEERING & TECHNOLOGY

SCHOOL OF ELECTRONIC SCIENCES

M.E- EMBEDDED SYSTEM TECHNOLOGY

PART TIME

AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY, PAIYANOOR

&

V.M.K.V. ENGINEERING COLLEGE, SALEM

CHOICE BASED CREDIT SYSTEM

2012 REGULATION
### I SEMESTER

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AIM:
Mathematics is fundamental for any field of technology. The aim of the subject is to impart essential mathematical topics for the PG courses in Electronics and Communication Engineering Department.

OBJECTIVE:
- To understand the concepts of fuzzy logic.
- To make the student learn different matrix methods and some of the applications.
- To understand the concepts of random variables.
- To make the student learn dynamic programming and their applications.
- To understand the concepts of different queuing models.

UNIT I: FUZZY LOGIC
Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II: MATRIX THEORY

UNIT III: ONE DIMENSIONAL RANDOM VARIABLES

UNIT IV: DYNAMIC PROGRAMMING

UNIT V: QUEUEING MODELS

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS
REFERENCES:

AIM:
Learning design of digital circuits is a fundamental necessity for designing embedded systems. This subject provides necessary instruments to achieve that goal.

OBJECTIVE:
To make the student learn: theory of logic and logic functions, design of digital circuits, and an introduction to VHDL language.

UNIT I: ADVANCED TOPICS IN BOOLEAN ALGEBRA
Shannon's expansion theorem, Conensus theorem, Octal designation, Run measure, INHIBIT / INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

UNIT II: THRESHOLD LOGIC
Linear sepeability, Unateness, Physical implementation, Dual comparability, reduced functions, various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

UNIT III: SYMMETRIC FUNCTIONS
Elementary symmetric functions, partially symmetric and totally symmetric functions, Mc Cluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

UNIT IV: SEQUENTIAL LOGIC CIRCUITS
Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

UNIT V: PROGRAMMABLE LOGIC DEVICES
Basic concepts, Programming technologies, Programmable Logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Structure of Standard PLD's, Complex PLD's (CPLD). System Design Using PLD's - Design of combinational and sequential circuits using PLD's, Programming PAL device using PALASM, Design of state machine using Algorithmic State Machines (ASM) chart as a design tool. Introduction To Field Programmable Gate Arrays - Types of FPGA, Xilinx XC3000 series, Logic Cell array (LCA), Configurable Logic Blocks (CLB) Input/Output Block (IOB)- Programmable Interconnect Point (PIP), Introduction to Actel ACT2 family and Xilinx XC4000 families, Design examples.

TOTAL: 45 HOURS

REFERENCES:
AIM:
The use of real time operating systems has become a necessity to build complex embedded systems, this subject is provided.

OBJECTIVE:
To make the student learn fundamentals of Operating Systems, implementation aspects of real time concepts and few applications on RTOS.

UNIT I: REVIEW OF OPERATING SYSTEMS

UNIT II: OVERVIEW OF RTOS
RTOS Task and Task state - Process Synchronisation- Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronisation problem – Deadlocks -

UNIT I II: REAL TIME MODELS AND LANGUAGES
Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT I V: REAL TIME KERNEL

UNIT V: RTOS APPLICATION DOMAINS

TOTAL: 45 HOURS

REFERENCES:
AIM:
This course aims to give the knowledge for students on all aspects of the design and development of an embedded system, including hardware and embedded software development.

OBJECTIVE:
At the end of this course the student can utilizes and applies the skills and knowledge upon embedded hardware as well as software development.

UNIT I: EMBEDDED DESIGN LIFE CYCLE  9

UNIT II: PARTITIONING DECISION  9

UNIT III: INTERRUPT SERVICE ROUTINES 9
Watch dog timers – Flash Memory basic toolset – Host based debugging – Remote debugging – ROM emulators – Logic analyser – Caches – Computer optimisation – Statistical profiling

UNIT IV: IN CIRCUIT EMULATORS 9

UNIT V: TESTING 9

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS
REFERENCES:

AIM:
To introduce concepts of data communication networks.

OBJECTIVE:
To make the student learn, all parts of communication software in layered architecture.

UNIT I OVERVIEW OF COMPUTER NETWORKS AND APPLICATION LAYER PROTOCOLS
An introduction to internet - An overview of circuit switching - Packet switching and message switching - Routing in data networks - Access networks and physical media - Protocol; layers - Comparison of OSI and Internet protocol stack - Internet backbones - Network access points and ISPS, Application layer protocols - Service provided by the Internet transport protocols – Network applications: www - Overview of HTTP - HTTP message format - User server interaction – Web caches FTP - FTP commands and replies - Electronic mail in the internet - SMPT, MIME – Mail access protocols - POP3 DNS - Introduction to socket programming with TCP and UDP.

UNIT II TRANSPORT LAYER PROTOCOLS
Transport layer services and principles - Relationship between transport and network layers - Overview of transport layer in the internet - Multiplexing and demultiplexing applications connectionless and connection oriented transports - Principles of reliable data transfer – Principles of congestion control.

UNIT III NETWORK LAYER

UNIT IV DATA LINK AND MAC LAYER
Data link layer services and adapters - Error detection and correction techniques – Multiple Access protocols and LANs - LAN addresses and ARP - Ethernet - Hubs - Bridges and Switches PPP- ATM- X.2.5 and Frame relay.
UNIT V NETWORK SECURITY AND MULTIMEDIA

Networks security - Principles of cryptography - Authentication - Integrity - Key distribution and certification - Secure Email - Internet commerce - Network layer security - Multimedia networking application - Streaming stored audio and video - Internet phone - Case study - RTP.

TOTAL: 45 HOURS

REFERENCES

3. T.N.Saadavi,M.H.Ammar & AL . Halleem” Fundamentals of Telecommunication Networks “ -
LIST OF EXPERIMENTS

1. Design with 8 bit Microcontrollers 8051/PIC Microcontrollers
   i) I/O Programming, Timers, Interrupts, Serial port programming
   ii) PWM Generation, Motor Control, ADC/DAC, LCD and RTC Interfacing, Sensor Interfacing
   iii) Both Assembly and C programming
2. Design with 16 bit processors
   I/O programming, Timers, Interrupts, Serial Communication,
3. Design with ARM Processors.
   I/O programming, ADC/DAC, Timers, Interrupts,
4. Study of one type of Real Time Operating Systems (RTOS)
5. Electronic Circuit Design of sequential, combinational digital circuits using CAD Tools
6. Simulation of digital controllers using MATLAB/LabVIEW.
7. Programming with DSP processors for Correlation, Convolution, Arithmetic adder, Multiplier, Design of Filters - FIR based, IIR based
8. Design with Programmable Logic Devices using Xilinx/Altera FPGA and CPLD
   Design and Implementation of simple Combinational/Sequential Circuits
9. Network Simulators
   Simple wired/wireless network simulation using NS2

TOTAL: 30 HOURS

REFERENCES:

3. Jan Axelson ‘Embedded Ethernet and Internet Complete’, Penram publications
AIM:
Any Embedded design mostly involves processor systems, this course describes computer architectures.

OBJECTIVES:
- At the end of this course the student will know various parallel processing applications and their performance towards real time computing.
- To impart knowledge on scalable architectures and the performances.

UNIT I- THEORY OF PARALLELISM, PARTITIONING AND SCHEDULING 9
Parallel Computer models: The state of computing, Multiprocessors and Multicomputers, Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks.
Program and network properties: Conditions of parallelism, Program partitioning and scheduling, program flow mechanisms, System interconnect architectures.

UNIT II- SCALABLE PERFORMANCES & HARDWARE TECHNOLOGIES 9
Principles of scalable performance: Performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.
Processor and memory hierarchy: Advanced processor technology, Superscalar and vector processors, memory hierarchy technology, virtual memory technology.

UNIT III- MEMORY ORGANIZATIONS & PIPELINING 9
Bus cache and shared memory: backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.
Pipelining: Linear and non-Linear Pipeline processors-Instruction pipeline design and Arithmetic pipeline design.

UNIT IV- PARALLEL & SCALABLE ARCHITECTURES 9
Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V- SOFTWARE & PARALLEL PROCESSING 9
Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL: 45 HOURS

TEXT BOOKS:

REFERENCE BOOKS:
AIM:
To introduce some C concepts relevant to embedded systems with 80x86 family as basis and UML.

OBJECTIVE:
To make the student learn: use of C language for embedded applications, real time UML concepts, co-design methods.

UNIT I  LOW LEVEL PROGRAMMING IN C

UNIT II  C AND ASSEMBLY

UNIT III  OBJECT-ORIENTED ANALYSIS AND DESIGN

UNIT IV  UNIFIED MODELLING LANGUAGE

UNIT V  CASE STUDIES

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:
2. Hassan Gomma, “Designing Concurrent, Distributed, and Real-Time applications with UML.
AIM:
This course will introduce approaches and methodologies for VLSI architectures of signal processing.

OBJECTIVE:
- At the end of this course the student can have knowledge about the basic approaches and methodologies for VLSI architectures of signal processing.
- The students will also have hands-on VLSI system design experience using hardware description language (HDL) and commercial EDA tools (Synopsys).

UNIT I  INTRODUCTION
Overview of digital VLSI design methodologies - Trends in IC technology – advanced Boolean algebra - Shannon’s expansion theorem - consensus theorem - Octal designation - Run measure - Buffer gates - Gate Expander - Reed Muller expansion - Synthesis of multiple output combinational logic circuits by product map method - Design of static hazard free and dynamic hazard free logic circuits.

UNIT II  ANALOG VLSI AND HIGH SPEED VLSI
Introduction to analog VLSI - Realisation of Neural networks and switched capacitor filters - sub-micron technology and GaAs VLSI technology.

UNIT III  PROGRAMMABLE ASICS
Anti fuse – static RAM – EPROM and EEPROM technology - PREP bench marks –Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC & AC inputs and outputs-clock and power inputs - Xilinx I/O blocks.

UNIT IV  PROGRAMMABLE ASIC DESIGN SOFTWARE

UNIT V  LOGIC SYNTHESIS, SIMULATION AND TESTING
Basic features of VHDL language for behavioural modelling and simulation - Summary of VHDL data types – dataflow and structural modelling – VHDL and logic synthesis – types of simulation – boundary scan test-fault simulation – automatic test pattern generation

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:
2. Amar Mukherjee, Introduction to NMOS and CMOS VLSI system design, Prentice hall 1986

Semester III
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<thead>
<tr>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>VLSI ARCHITECTURE AND DESIGN METHODOLOGIES</td>
<td>3</td>
<td>1</td>
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AIM:
This course aims to provide students with an understanding of digital image processing techniques, including image reconstruction and restoration, segmentation and enhancement, also colour and morphological image processing techniques.

OBJECTIVE:
Upon successful completion of this course, students should be able to understand all types of image processing techniques.

UNIT I: INTRODUCTION TO IMAGE PROCESSING SYSTEMS & IMAGETRANSFORMS

Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Applications of Digital image processing

Introduction, Need for transform, Image transforms, Fourier transform, 2 D Discrete Fourier transform and its transforms, Importance of phase, Walsh transform, Hadamard transform, Haar transform, slant transform Discrete cosine transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms.

UNIT II: IMAGE ENHANCEMENT & IMAGE RESTORATION

Introduction to image enhancement, Enhancement in spatial domain, enhancement through point operation, Types of point operation, Histogram manipulation, Linear Gray level transformation, Nonlinear Gray level transformation, Local or neighbourhood operation, Median filter, Image sharpening, Bit plane slicing, Image enhancement in the frequency domain.

Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution

UNIT III: IMAGE SEGMENTATION AND IMAGE COMPRESSION

Introduction to image segmentation, Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour

UNIT IV: COLOUR IMAGE PROCESSING
9
Introduction, Light and colour, colour formation, Human perception of colour, colour model The chromaticity diagram, colour image quantization, Histogram of colour image, colour image filtering, Gamma correction of a colour image, colour image segmentation.

UNIT V: MORPHOLOGICAL IMAGE PROCESSING
9
Preliminaries-Dilation & Erosion, Opening & Closing, Hit or Miss Transformation, Basic Morphological Algorithms, Extension to Gray scale Images.

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:
1. ATMEL CPLDs – Prochip designer
   a) Schematic entry
   b) VHDL entry
2. AT40K FPGA series – synthesis – design – simulation of application programs
3. Xilinx EDA design tools – device programming – PROM programming
4. ALTERA and Mentor graphics – IC design tools
5. Code compressor studio for embedded DSP using Texas tool kit
6. Cell based ASICs – sample programs for risk and security plans
7. IPCORE usage in VOIP through SoC2 tools
8. FPSLIC synthesis testing and examples
9. Third party tools for embedded java and embedded C++ applications through cadence tools.

TOTAL: 30 HOURS
AIM:

As VLSI implementation is largely in ASIC, this subject is introduced here.

OBJECTIVE:

To make the student learn the fundamentals of ASIC and its design methods.

UNIT I  INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN

Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture

UNIT II  PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS

PROGRAMMABLE ASIC I/O CELLS

Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinxce 08 I/O blocks.

UNIT III  PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY


UNIT IV  LOGIC SYNTHESIS, SIMULATION AND TESTING

Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V  ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL: 45 HOURS
REFERENCES:

AIM:
The aim of this course is to develop and deploy advances in measurement science to safely increase the versatility, autonomy, and rapid re-tasking of intelligent robots and automation technologies.

OBJECTIVE:
At the end of this course student will infer some knowledge regarding advanced robotics and automation.

UNIT I INTRODUCTION
Geometric configuration of robots - manipulators - drive systems - internal and external sensors - end effectors - control systems - robot programming languages and applications - Introduction to robotic vision.

UNIT II ROBOT ARM KINEMATICS
Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation - Denavit Hattenberg representation and various arm configurations.

UNIT III ROBOT ARM DYNAMICS
Lagrange - Euler formulation, joint velocities - kinetic energy - potential energy and motion equations – generalized D'Alembert equations of motion.

UNIT IV ROBOT APPLICATIONS

UNIT V ASSEMBLY AND INSPECTION
Assembly and robotic assembly automation – Parts presentation methods – assembly operation – Compliance and the Remote Center Compliance(RCC) device – Assembly system Configurations – Adaptable, Programmable assembly system – Designing for robotic assembly – Inspection automation.

TOTAL: 45 HOURS

REFERENCES:
AIM
The purpose of Video Processing course is to cover the fundamentals of digital video signal generation and further processing over the communication systems.

OBJECTIVE
To learn the basic concepts of video processing
To learn about the various methodologies for motion estimation
To learn the basic concepts of coding systems
To understand about the waveform based video coding techniques
To understand about the content dependent and scalable video coding techniques

UNIT I VIDEO FORMATION, PERCEPTION AND REPRESENTATION 9

UNIT II TWO-DIMENSIONAL MOTION ESTIMATION 9
General Methodologies, Pixel-Based Motion Estimation, Block Matching Algorithm, Mesh-based Motion estimation, Global Motion Estimation, Region –Based Motion Estimation, Multiresolution Motion Estimation, Application of Motion Estimation in Video Coding.
Feature-based Motion Estimation.

UNIT III FOUNDATIONS OF VIDEO CODING 9
Overview of Coding Systems, Basic Notions in Probability and Information Theory, Information Theory for Source Coding, Binary Encoding, Scalar Quantization, Vector Quantization.

UNIT IV WAVEFORM-BASED VIDEO CODING 9
Block-Based Transform Coding, Predictive Coding, Video Coding Using Temporal Prediction and Transform Coding.

UNIT V CONTENT-DEPENDENT & SCALABLE VIDEO CODING 9
Two-Dimensional Shape Coding, Texture coding for Arbitrarily Shaped Regions, Joint Shape & Texture Coding, Region-Based Video Coding, Object-based Video Coding. Basic Modes of Scalability, Object Based Scalability, Wavelet-transform Based Coding.

TOTAL HOURS: 45

TEXT BOOKS:

REFERENCES:
AIM:
This course aims to provide the student to apply engineering knowledge and specialist techniques to prevent or to reduce the likelihood or frequency of failures.

OBJECTIVE:
The students will be able to understand the ways in which product fail, the effects of failure and aspects of design, manufacture, maintenance and use which affect the likelihood of failure.

UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE 9
Statistical distribution, statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference, Safety margin and loading roughness on reliability.

UNIT II RELIABILITY PREDICTION, MODELLING AND DESIGN 9
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY 9
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design, software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS 9
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MANAGEMENT 9
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

TOTAL: 45 HOURS

REFERENCES:
York, 1998
AIM:
To understand different electromagnetic Interference problems occurring in Intersystem and in inter system and their possible mitigation techniques in Electronic design.

OBJECTIVES:
➢ To understand EMI Sources, EMI problems and their solution methods in PCB level / Subsystem and system level design.
➢ To measure the emission immunity level from different systems to couple with the prescribed EMC standards.

UNIT I  EMI/EMC CONCEPTS
EMI- EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II  EMI COUPLING PRINCIPLES
Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES
Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBS
Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS
Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

TOTAL: 45 HOURS

REFERENCES:
AIM:
To expose students to the advanced digital signal processing systems for VLSI and associated EDA Tools.

OBJECTIVE:
At the end of this course the student will be able knowing methods and techniques for implementation of DSP systems.

UNIT I  INTRODUCTION TO DSP SYSTEMS  9
Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II  RETIMING  9
Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge-Sort architecture, parallel rank-order filters.

UNIT III  FAST CONVOLUTION  9

UNIT IV  BIT-LEVEL ARITHMETIC ARCHITECTURES  9
Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement.

UNIT V  PROGRAMMING DIGITAL SIGNAL PROCESSORS  9
Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low
power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

TOTAL: 45 HOURS

REFERENCES:
AIM
To produce the knowledge on cyber security essentials

OBJECTIVE
- To study the cyber security fundamentals
- To study the various techniques on attack and exploitation
- To study in detail about malicious code
- To study about defense and analysis techniques

UNIT I CYBER SECURITY FUNDAMENTALS


UNIT II ATTACKER TECHNIQUES AND MOTIVATIONS

Antiforensics – Tunneling techniques – Fraud Techniques - Threat Infrastructure.

UNIT III EXPLOITATION

Techniques to gain a foot hold – Misdirection, Reconnaissance, and disruption methods.

UNIT IV MALICIOUS CODE


UNIT V DEFENSE AND ANALYSIS TECHNIQUES


TOTAL HOURS: 45

TEXT BOOK

REFERENCE BOOKS
AIM:
Main aim of this course is to make the students understand in identifying and analyzing the requirements that a distributed multimedia application may enforce on the communication network.

OBJECTIVE:
At the end of this course students have knowledge in distributing multimedia application over the communication network.

UNIT I MULTIMEDIA NETWORKING
Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video.

UNIT II BROAD BAND NETWORK TECHNOLOGY
Broadband services, ATM and IP , IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance.

UNIT III MULTICAST AND TRANSPORT PROTOCOL
Multicast over shared media network, multicast routing and addressing, scaping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP.

UNIT IV MEDIA - ON – DEMAND
Storage and media servers, voice and video over IP, MPEG over ATM/IP, indexing synchronization of requests, recording and remote control.

UNIT V APPLICATIONS
MIME, Peer-to-peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy.

TOTAL HOURS: 45

REFERENCES:
AIM: This course is intended to introduce the student to learn about Device Modeling—Various types of analog systems—CMOS amplifiers and Comparators.

OBJECTIVE:
By the end of the term, students should be able to:

- Demonstrate an understanding of MOS terminal characteristics and capacitive effects.
- Create integrated circuit layouts showing an awareness of the underlying process technology and layout parasitic as well as their impact on circuit performance.

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT-Mode SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING
Continuous-Time Signal Processing—Sampled-Data Signal Processing—Switched-CURRENT Data Converters—Practical Considerations in SI Circuits—Biologically-Inspired Neural Networks —Floating-Gate, Low-Power Neural Networks—CMOS Technology and Models—Design Methodology—Networks—Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS
UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT


TOTAL: 45 HOURS

REFERENCES:
AIM:
As there is always a need for power efficient circuits and devices, this course explain the methods for low power VLSI design.

OBJECTIVE:
At the end of this course the student will be able to design Low power CMOS designs, for digital circuits.

UNIT I
Introduction - Simulation - Power Analysis-Probabilistic Power Analysis.

UNIT II

UNIT III

UNIT IV

UNIT V

TOTAL: 45 HOURS

REFERENCES:
AIM:
To provide knowledge on basic embedded drivers, embedded Linux and their functioning.

OBJECTIVE:
To study embedded linux and their device drivers functioning and applications.

UNIT I FUNDAMENTALS OF OPERATING SYSTEMS 9

UNIT II LINUX FUNDAMENTALS 9
Introduction to Linux – Basic Linux commands and concepts – Logging in - Shells - Basic text editing - Advanced shells and shell scripting – Linux File System – Linux programming - Processes and threads in Linux - Inter process communication – Devices – Linux System calls

UNIT III INTRODUCTION TO EMBEDDED LINUX 9
Embedded Linux – Introduction – Advantages- Embedded Linux Distributions - Architecture - Linux kernel architecture - User space – linux startup sequence - GNU cross platform Tool chain

UNIT IV BOARD SUPPORT PACKAGE AND EMBEDDED STORAGE 9

UNIT V EMBEDDED DRIVERS AND APPLICATION PORTING 9

TOTAL: 45 HOURS

REFERENCE BOOKS

AIM:
The aim of this course is provide an introduction of an advanced element of learning in the field of wireless communication and also expose the students to the concepts of wireless devices and mobile computing.

OBJECTIVE:
At the end of this course the student should be able to understand the concept of mobile computing and architecture of mobile communication.

UNIT I INTRODUCTION
Basics of mobile computing - Medium access control – Telecommunication systems – Satellite systems – Broadcast systems.

UNIT II STANDARDS
Wireless LAN – IEEE 802.11 – Frequency Hopping spread spectrum – Direct sequence and spread spectrum - HIPERLAN – Bluetooth.

UNIT III ADHOC NETWORKS

UNIT IV NETWORK ISSUES

UNIT V APPLICATION ISSUES

TOTAL: 45 HOURS

REFERENCES:
AIM:
Since the concepts of real time systems and their analysis is very essential for embedded students this subject is given.

OBJECTIVE:
To make the student learn, all real time aspects of various system components, like OS, memory, communication and an introduction to reliability evaluation methods.

UNIT I  INTRODUCTION  9
Introduction - issues in real time computing - structure of a real time system - task classes - performance measures for real time systems - estimating program run times - task assignment and scheduling - classical uniprocessor scheduling algorithms - uniprocessor scheduling of IRIS tasks - tasks assignment - mode changes - fault tolerant scheduling.

UNIT II  PROGRAMMING LANGUAGES AND TOOLS  9
Language features - desired language characteristics - data typing - control structures - facilitating hierarchical decomposition - package - run-time error handling - overloading and generics - multitasking - low level programming - task scheduling - timing specifications - programming environments - run-time support – code generation.

UNIT III  REAL TIME DATABASES  9
Real time database - basic definition - real time Vs general-purpose database - main memory databases - transaction priorities - transaction aborts - concurrency control issues - disk scheduling algorithms - two-phase approach to improve predictability - maintaining serialization consistency - databases for hard real time systems.

UNIT IV  COMMUNICATION  9

UNIT V  EVALUATION TECHNIQUES  9
Reliability evaluation techniques - reliability models for hardware redundancy - software error models – response time calculation – interrupt latency – time loading and its measurement – reducing response times – analysis of memory requirements – reducing memory loading

TOTAL: 45 HOURS

TEXT BOOK:


REFERENCES:


AIM:
To enhance the knowledge of the student about basic embedded architectures and their applications of high end processors.

OBJECTIVE:
- To study basic processor accessories.
- To study DSP & ARM Processors and their applications.

UNIT I INTRODUCTION

UNIT II ANALOG DSP

UNIT III ARM PROCESSOR
Introduction, architecture, instruction set, addressing modes, applications – Palm One OS5-based device with ARM processor – ARM application processor – ARM720T and ARM920T.

UNIT IV OPEN MULTIMEDIA APPLICATION PLATFORM
Introduction, architecture, instruction set, addressing modes, applications – OMAP5910 –module overview, display specification, LCD controller operation, Lookup palette, color dithering, output FIFO, LCD controller pins, LCD controller registers, interface to LCD panel signal reset values.

UNIT V CASE STUDY
Audio/video and VOIP application for multimedia application using OMAP TI-5012 – TI OMAP Applications Processor - OMAP2420 and OMAP1710 – architecture, features and applications.

TOTAL: 45 HOURS

TEXT BOOK:

REFERENCE BOOKS:
AIM:
This course aims to make students understand basic current mixed signal systems, circuit building blocks, basic operation method and design method.

OBJECTIVE:
At the end of the course the students will be provided with a unified view of physical system architectures from chip, circuit board, to cabinets. They will also have knowledge on basic theory and analysis methods as well as design practice for high performance interconnections and packaging in such complex, mixed-signal end-products as mobile terminals and base-stations.

UNIT I INTRODUCTION TO ANALOG AND MIXED SIGNAL CIRCUITS 9

UNIT II CMOS AMPLIFIERS 9
Opamps - High Performance CMOS amplifiers – Comparators – Characterization - Two stage open loop comparators - Discrete time comparators - High-speed comparators.

UNIT III SWITCHED CAPACITOR CIRCUITS 9
Switched Capacitor (SC) Introduction - offset cancellation - clock feed - through - Switched Capacitor amplifiers - Switched Capacitor Integrators - Switched Capacitor filters.

UNIT IV DATA CONVERTERS 9
Introduction - Nyquist rate converters – Over sampling converters - Pipelined/parallel converters - High speed ADC design, High speed DAC design and Mixed signal design for radar application - ADC and DAC modules used for LIGO.

UNIT V PHASE LOCKED LOOPS 9

TEXT BOOKS:

REFERENCE BOOKS:
AIM:
To introduce the basic concepts of control systems and its embedded implementation.

OBJECTIVE:
To make the student learn, basics of control systems, application methods of control theory in embedded systems.

UNIT I  INTRODUCTION  9
Controlling the hardware with software – data lines – numbering systems – address lines - ports – schematic representation – bit masking – programmable peripheral interface – switch input detection.

UNIT II  INPUT-OUTPUT DEVICES  9

UNIT III  D/A AND A/D CONVERSION  9
R 2R ladder - more on Op-Amps - virtual ground - resistor network analysis - port offsets - triangle waves analog vs digital values - ADC0809 – comparator - successive approximation - the ADC clock - ripple counter - D flip-flop - Q and NOT Q - aliasing – multiplexer - Auto port detect - recording and playing back voice - capturing analog information in the timer interrupt service routine - automatic, multiple channel analog to digital data acquisition.

UNIT IV  ASYNCHRONOUS SERIAL COMMUNICATION  9

UNIT V  CASE STUDIES  9

TOTAL: 45 HOURS

REFERENCES:

AIM:
This course is an introduction to MEMS, which also uses micro electronics. This course fulfills the need of electronic engineer who want to create MEMS devices.

OBJECTIVE:
At the end of this course, the student will have knowledge on MEMS materials, fabrication and micro sensor design.

UNIT I INTRODUCTION

UNIT II MICROSENSING FOR MEMS

UNIT III MICRO MACHINING
Micromachning : Bulk micromachining for silicon-based MEMS -Isotropic and orientation-dependent wet etching- Dry etching -Buried oxide process -Silicon fusion bonding -Anodic bonding -Silicon surface micromachining Sacrificial layer technology - Material systems in sacrificial layer technology - Surface micromachining using plasma etching-Combined integrated-circuit technology and anisotropic wet etching.

UNIT IV LITHOGRAPHY

UNIT V APPLICATIONS
Switching: Introduction- Switch parameters- Basics of switching - Mechanical switches-Electronic switches-Switches for RF and microwave applications - Mechanical RF switches - PIN diode RF switches

TEXT BOOK:

TOTAL: 45 HOURS

REFERENCE BOOKS:
5. N Maluf An Introduction to Microelectromechanical Systems Engineering, Artech House
AIM:
This course will provide a comprehensive and structured exposure to Soft Computing Techniques i.e Artificial Neural Networks, Fuzzy Logic, Genetic Algorithm, Particle Swarm Optimization.

OBJECTIVE:
To make the student learn, all types of soft computing techniques and how it is applied in various fields.

UNIT I  INTRODUCTION

UNIT II  ARTIFICIAL NEURAL NETWORKS

UNIT III  FUZZY LOGIC SYSTEM
Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning. Introduction to fuzzy logic modeling and control. Fuzzification, inferencing and defuzzification. Fuzzy knowledge and rule bases. Fuzzy modeling and control schemes for nonlinear systems. Self-organizing fuzzy logic control. Fuzzy logic control for nonlinear time-delay system.

UNIT IV  GENETIC ALGORITHM
Basic concept of Genetic algorithm and detail algorithmic steps, adjustment of free parameters. Solution of typical control problems using genetic algorithm. Concept on some other search techniques like tabu search and ant-colony search techniques for solving optimization problems.

UNIT V  APPLICATIONS

TOTAL: 45 HOURS

REFERENCES
AIM:

The aim of the course is to teach students to use digital signal processors such as the TMS320C6xxx to perform real-time DSP on real signals.

OBJECTIVE:

This course brings together some of the theory and understanding you have gained in several other lecture courses and lets you apply that theory in solving the type of problem which might be encountered by a DSP engineer in industry.

UNIT I: FUNDAMENTALS OF PROGRAMMABLE DSP'S

UNIT II: TMS320C5X PROCESSOR
Architecture – Assembly Language syntax- Addressing modes- Assembly language Instructions – pipeline structure, Operation – Block diagram of DSP Starter kit – Application Programs for processing real time signals.

UNIT III: TMS320C3X PROCESSOR
Architecture – Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation – Block diagram of DSP starter kit – Application, Programs for processing real time systems – Generating and finding the sum of series, Convolution of two sequences, Filter design.

UNIT IV: ADSP PROCESSORS
Architecture of ADSP-21XX and ADSP – 210XX series of DSP processors – Addressing modes and Assembly language instructions – Applications programs – Filter design, FFT calculation- Blackfin DSP Processor

UNIT V: ADVANCED PROCESSORS

TOTAL: 45 HOURS

TEXT BOOK:


REFERENCES:

1. User guides Texas Instrumentation, Analog Devices, Motorola.
AIM:
This course aims to provide in depth knowledge to students about the artificial neural networks and also Fuzzy Logic as well as application of it.

OBJECTIVE:
- To make the student learn to improve their skills over artificial neural network and their application.
- To make the student learn to understand the concepts of fuzzy logic and their application.

UNIT I FUNDAMENTALS OF ANN

UNIT II ANN ALGORITHM

UNIT III APPLICATION OF ANN

UNIT IV INTRODUCTION TO FUZZY LOGIC

UNIT V APPLICATION OF FUZZY LOGIC

REFERENCES:
1. Freeman & Skapura, “Neural Networks”, Addison - Wesley, 1991
AIM:

To enhance the knowledge of student with various algorithms and techniques to apply in controllers.

OBJECTIVE:

- To study the basic digital control system design and its stability testing.
- To study the models of digital devices and systems.
- To learn about digital control algorithms.
- To study about control systems analysis using state variable methods.
- To analyse the control systems using state variable methods.

Unit I Digital Control, Signal Processing in digital control


Unit II Models of Digital Control Devices and Systems


Unit III Design of digital Control Algorithms


Unit IV Control System analysis using state Variable Methods


Unit V Practical Aspects of Digital Control Algorithms

Mechanisation of control Algorithms using Microprocessors – Microprocessor Based Temperature Control Systems–Case Study – Stepping Motors and their Interfacing to Microprocessors

TOTAL HOURS: 45

Text Books


Reference Books:
AIM:
As now embedded systems has to be designed with some communication facility to give interaction between themselves and multi processing systems work in a distributed environment this course on distributed embedded systems is included in the curriculum.

OBJECTIVE:
To make the student learn: distributed system concepts, JAVA programming and some design concepts related to distributed systems.

UNIT I       THE HARDWARE INFRASTRUCTURE    9

UNIT II      INTERNET CONCEPTS      9
Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

UNIT III     DISTRIBUTED COMPUTING USING JAVA   9

UNIT IV     EMBEDDED AGENT      9

UNIT V       EMBEDDED COMPUTING ARCHITECTURE   9

TOTAL: 45 HOURS

REFERENCES: