VINAYAKA MISSIONS UNIVERSITY, SALEM

TAMILNADU, INDIA.

FACULTY OF ENGINEERING & TECHNOLOGY

SCHOOL OF ELECTRONIC SCIENCES

M.E- EMBEDDED SYSTEM TECHNOLOGY

PART TIME

AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY, PAIYANOOR

&

V.M.K.V. ENGINEERING COLLEGE, SALEM

CHOICE BASED CREDIT SYSTEM

2012 REGULATION

I SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
	THEORY					
1	Applied Mathematics for Electronics Engineers	MATHS	3	1	0	4
2	Advanced Digital System Design	ECE	3	0	0	3
3	Real Time Operating Systems	ECE	3	0	0	3
	TOTAL					10

II SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
	THEORY					
1	Design of Embedded Systems	ECE	3	1	0	4
2	Data Communication & Networks	ECE	3	0	0	3
3	Elective I	ECE	3	0	0	3
	PRACTICAL					
4	Embedded Systems Lab I	ECE	0	0	2	2
	TOTAL					12

III SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
	THEORY					
1	Computer Architecture & Parallel Processing	CSE	3	0	0	3
2	Software Technology for Embedded Systems	ECE	3	1	0	4
3	VLSI Architecture and Design methodologies	ECE	3	1	0	4
	TOTAL					11

IV SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Advanced Digital Image Processing	ECE	3	1	0	4
2	Elective II	ECE	3	0	0	3
3	Elective III	ECE	3	0	0	3
PRACTICAL						
4	Embedded Systems Lab II	ECE	0	0	0	2
TOTAL						12

V SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
THEORY						
1	Elective IV	ECE	3	0	0	3
2	Elective V	ECE	3	0	0	3
3	Elective VI	ECE	3	0	0	3
PRACTICAL						
4	Project Work Phase I	ECE	0	0	6	6
TOTAL						15

VI SEMESTER

S.No.	Course Title	Offering Department	L	T	P	C
PRACTICAL						
1	Project Work Phase II	ECE	0	0	12	12
TOTAL						12

Overall Credits

S.No	Semester	Credits
1	I	10
2	II	12
3	III	11
4	IV	12
5	V	15
6	V1	12
Total		72

ELECTIVES LIST

S.No.	Course Title	Offering Department	L	T	P	C
1	ASIC Design	ECE	3	0	0	3
2	Advanced Robotics & Automation	ECE	3	0	0	3
3	Video Processing	ECE	3	0	0	3
4	Reliability Engineering for Electronics	ECE	3	0	0	3
5	Electromagnetic Interference & Compatibility	ECE	3	0	0	3
6	VLSI Signal Processing	ECE	3	0	0	3
7	Cyber Security	CSE	3	0	0	3
8	Internetworking Multimedia	CSE	3	0	0	3
9	Analog VLSI Design	ECE	3	0	0	3
10	Low Power VLSI Design	ECE	3	0	0	3
11	Embedded Linux	ECE	3	0	0	3
12	Mobile Computing	ECE	3	0	0	3
13	Real Time Systems	ECE	3	0	0	3
14	Embedded Processors	ECE	3	0	0	3
15	Mixed Signal System	ECE	3	0	0	3
16	Embedded Control Systems	ECE	3	0	0	3
17	MEMS	ECE	3	0	0	3
18	Soft Computing Techniques	CSE	3	0	0	3
19	DSP Processors	ECE	3	0	0	3
20	Fuzzy Logic & Artificial Intelligence	CSE	3	0	0	3
21	Digital Control Engineering	EEE	3	0	0	3
22	Distributed Embedded Computing	ECE	3	0	0	3

	SEMESTER I	L	T	P	C
	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS	**3**	**1**	**0**	**4**

AIM:

Mathematics is fundamental for any field of technology. The aim of the subject is to impart essential mathematical topics for the PG courses in Electronics and Communication Engineering Department.

OBJECTIVE:

➢ To understand the concepts of fuzzy logic.

➢ To make the student learn different matrix methods and some of the applications.

➢ To understand the concepts of random variables.

➢ To make the student learn dynamic programming and their applications.

➢ To understand the concepts of different queuing models.

UNIT I: FUZZY LOGIC 9

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II: MATRIX THEORY 9

Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition - Toeplitz matrices and some applications.

UNIT III: ONE DIMENSIONAL RANDOM VARIABLES 9

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform,

Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV: DYNAMIC PROGRAMMING 9

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V: QUEUEING MODELS 9

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:

1. George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 1997.
2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2000.
3. Richard Johnson, Miller & Freund's Probability and Statistics for Engineers, 7th Edition, Prentice – Hall of India, Private Ltd., New Delhi (2007).

4. Taha, H.A., Operations Research, An introduction, 7th edition, Pearson education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, Fundamentals of Queueing theory, 2nd edition, John Wiley and Sons, New York (1985).

	SEMESTER I	L	T	P	C
	ADVANCED DIGITAL SYSTEM DESIGN	**3**	**0**	**0**	**3**

AIM:

Learning design of digital circuits is a fundamental necessity for designing embedded systems. This subject provides necessary instruments to achieve that goal.

OBJECTIVE:

To make the student learn: theory of logic and logic functions, design of digital circuits, and an introduction to VHDL language.

UNIT I: ADVANCED TOPICS IN BOOLEAN ALGEBRA   9
Shannon's expansion theorem, Conseusus theorem, Octal designation, Run measure, INHIBIT / INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

UNIT II: THRESHOLD LOGIC   9
Linear seperability, Unateness, Physical implementation, Dual comparability, reduced functions, various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

UNIT III: SYMMETRIC FUNCTIONS   9
Elementary symmetric functions, partially symmetric and totally symmetric functions, Mc Cluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

UNIT IV: SEQUENTIAL LOGIC CIRCUITS   9
Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

UNIT V: PROGRAMMABLE LOGIC DEVICES   9
Basic concepts, Programming technologies, Programmable Logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Structure of Standard PLD's, Complex PLD's (CPLD). System Design Using PLD's - Design of combinational and sequential circuits using PLD's, Programming PAL device using PALASM, Design of state machine using Algorithmic State Machines (ASM) chart as a design tool. Introduction To Field Programmable Gate Arrays - Types of FPGA, Xilinx XC3000 series, Logic Cell array (LCA), Configurable Logic Blocks (CLB) Input/Output Block (IOB)- Programmable Interconnect Point (PIP), Introduction to Actel ACT2 family and Xilinx XC4000 families, Design examples.

TOTAL: 45 HOURS

REFERENCES:

1. William I. Fletcher, "An Engineering Approach to Digital Design" , Prentice Hall of India, 1996.
2. James E. Palmer, David E. Perlman, "Introduction to Digital Systems", Tata McGraw Hill, 1996.
3. N.N. Biswas, "Logic Design Theory", Prentice Hall of India, 1993.
4. S. Devadas, A. Ghosh and K. Keutzer, "Logic Synthesis", Mc Graw Hill, 1994.

Semester I	L	T	P	C
REAL TIME OPERATING SYSTEMS	**3**	**0**	**0**	**3**

AIM:

The use of real time operating systems has become a necessity to build complex embedded systems, this subject is provided.

OBJECTIVE:
To make the student learn fundamentals of Operating Systems, implementation aspects of real time concepts and few applications on RTOS.

UNIT I: REVIEW OF OPERATING SYSTEMS   9

Basic Principles - Operating System structures – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes –Introduction to Distributed operating system – Distributed scheduling.

UNIT II: OVERVIEW OF RTOS   9

RTOS Task and Task state - Process Synchronisation- Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronisation problem – Deadlocks -

UNIT I II: REAL TIME MODELS AND LANGUAGES   9

Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT I V: REAL TIME KERNEL   9

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

UNIT V: RTOS APPLICATION DOMAINS   9

RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

TOTAL: 45 HOURS

REFERENCES:

1. Raj Kamal, "Embedded Systems- Architecture, Programming and Design" Tata McGraw Hill, 2006.
 2. Herma K., "Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic, 1997.

3 Charles Crowley, "Operating Systems-A Design Oriented approach" McGraw Hill 1997.

4 C.M. Krishna, Kang, G.Shin, "Real Time Systems", McGraw Hill, 1997.

5. Raymond J.A.Bhur, Donald L.Bailey, "An Introduction to Real Time Systems", PHI 1999.

6. Mukesh Sighal and N G Shi "Advanced Concepts in Operating System", McGraw Hill   2000.

Semester II	L	T	P	C
DESIGN OF EMBEDDED SYSTEMS	3	1	0	4

AIM:

This course aims to give the knowledge for students on all aspects of the design and development of an embedded system, including hardware and embedded software development.

OBJECTIVE:

At the end of this course the student can utilizes and applies the skills and knowledge upon embedded hardware as well as software development.

UNIT I: EMBEDDED DESIGN LIFE CYCLE 9

Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing – Selection Processes – Microprocessor Vs Micro Controller – Performance tools – Bench marking – RTOS Micro Controller – Performance tools – Bench marking – RTOS availability – Tool chain availability – Other issues in selection processes.

UNIT II: PARTITIONING DECISION 9

Hardware / Software duality – coding Hardware – ASIC revolution – Managing the Risk – Co-verification – execution environment – memory organization – System startup – Hardware manipulation – memory mapped access – speed and code density

UNIT III: INTERRUPT SERVICE ROUTINES 9

Watch dog timers – Flash Memory basic toolset – Host based debugging – Remote debugging – ROM emulators – Logic analyser – Caches – Computer optimisation – Statistical profiling

UNIT IV: IN CIRCUIT EMULATORS 9

Buller proof run control – Real time trace – Hardware break points – Overlay memory – Timing constraints – Usage issues – Triggers.

UNIT V: TESTING 9

 Bug tracking – reduction of risks & costs – Performance – Unit testing – Regression testing – Choosing test cases – Functional tests – Coverage tests – Testing embedded software – Performance testing – Maintenance.

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

REFERENCES:

1. Arnold S. Berger – "Embedded System Design", CMP books, USA 2002.

2. Sriram V. Iyer, Pankaj Gupta, "Embedded Real-time Systems. Programming", Tata McGraw Hill, 2004.

3. ARKIN, R.C., Behaviour-based Robotics, The MIT Press, 1998.

Semester II	L	T	P	C
DATA COMMUNICATION AND NETWORKS	3	0	0	3

AIM:

To introduce concepts of data communication networks.

OBJECTIVE:

To make the student learn, all parts of communication software in layered architecture.

UNIT I OVERVIEW OF COMPUTER NETWORKS AND APPLICATION LAYER PROTOCOLS 9

An introduction to internet - An overview of circuit switching - Packet switching and message switching - Routing in data networks - Access networks and physical media - Protocol; layers - Comparison of OSI and Internet protocol stack - Internet backbones - Network access points and ISPS, Application layer protocols - Service provided by the Internet transport protocols – Network applications: www - Overview of HTTP - HTTP message format - User server interaction – Web caches FTP - FTP commands and replies - Electronic mail in the internet - SMPT, MIME – Mail access protocols - POP3 DNS - Introduction to socket programming with TCP and UDP.

UNIT II TRANSPORT LAYER PROTOCOLS 9

Transport layer services and principles - Relationship between transport and network layers - Overview of transport layer in the internet - Multiplexing and demultiplexing applications connectionless and connection oriented transports - Principles of reliable data transfer – Principles of congestion control.

UNIT III NETWORK LAYER 9

Datagram and virtual circuit service - Routing principles - Internet protocols IPVI Addressing and routing datagram format _ IP fragmentation and reassembly - ICMP routing in the internet - Router - Input ports - Switching fabrics - Output ports - Queuing - IPV6 packet format transition from IPV4 to IPV6 Multicast routing.

UNIT IV DATA LINK AND MAC LAYER 9

Data link layer services and adapters - Error detection and correction techniques – Multiple Access protocols and LANs - LAN addresses and ARP - Ethernet - Hubs - Bridges and Switches PPP- ATM-X.2.5 and Frame relay.

UNIT V NETWORK SECURITY AND MULTIMEDIA **9**

Networks security - Principles of cryptography - Authentication - Integrity - Key distribution and certification - Secure Email - Internet commerce - Network layer security - Multimedia networking application - Streaming stored audio and video - Internet phone - Case study - RTP.

TOTAL: 45 HOURS

REFERENCES

1. K.Kurose and K.W.Ross - "Computer network" Addison Wesley.(1997)
2. A.S . Tanenbaum "Computer Networks "- (3/e), (2001).
3. T.N.Saadavi,M.H.Ammar & AL . Halleem" Fundamentals of Telecommunication Networks " -
4. Wiley J.K.Buford - "Multimedia Systems" - Addison Wesley.(2001)

Semester II	L	T	P	C
EMBEDDED SYSTEMS LAB I	0	0	2	2

LIST OF EXPERIMENTS

1. Design with 8 bit Microcontrollers 8051/PIC Microcontrollers
   i) I/O Programming, Timers, Interrupts, Serial port programming
   ii) PWM Generation, Motor Control, ADC/DAC, LCD and RTC Interfacing, Sensor Interfacing
   iii) Both Assembly and C programming
2. Design with 16 bit processors
   I/O programming, Timers, Interrupts, Serial Communication,

3. Design with ARM Processors.
   I/O programming, ADC/DAC, Timers, Interrupts,

4. Study of one type of Real Time Operating Systems (RTOS)
5. Electronic Circuit Design of sequential, combinational digital circuits using CAD Tools
6. Simulation of digital controllers using MATLAB/LabVIEW.
7. Programming with DSP processors for
   Correlation, Convolution, Arithmetic adder, Multiplier, Design of Filters - FIR based , IIR based

8. Design with Programmable Logic Devices using Xilinx/Altera FPGA and CPLD
   Design and Implementation of simple Combinational/Sequential Circuits

9. Network Simulators
   Simple wired/ wireless network simulation using NS2

10. Programming of TCP/IP protocol stack.

TOTAL: 30 HOURS

REFERENCES:

1. Mohamammad Ali Mazidi & Mazidi ' 8051 Microcontroller and Embedded Systems', Pearson Education
2. Mohammad Ali Mazidi, Rolind Mckinley and Danny Causey, 'PIC Microcontroller and Embedded Systems' Pearson Education
3. Jan Axelson 'Embedded Ethernet and Internet Complete', Penram publications
4. Kraig Mitzner, 'Complete PCB Design using ORCAD Capture and Layout', Elsevier
5. Woon-Seng Gan, Sen M. Kuo, 'Embedded Signal Processing with the Micro Signal Architecture', John Wiley & Sons, Inc., Hoboken, New Jersey 2007
6. U. Meyer-Baese 'Digital Signal Processing using Field Programmable Gate Arrays', Springer
7. Dogan Ibrahim, 'Advanced PIC microcontroller projects in C', Elsevier 2008

Semester III	L	T	P	C
COMPUTER ARCHITECTURE & PARALLEL PROCESSING	**3**	**0**	**0**	**3**

<div align="center">(Common to Applied Electronics and VLSI Design)</div>

AIM:
Any Embedded design mostly involves processor systems, this course describes computer architectures.

OBJECTIVES:
- At the end of this course the student will know various parallel processing applications and their performance towards real time computing.

- To impart knowledge on scalable architectures and the performances.

UNIT I- THEORY OF PARALLELISM, PARTITIONING AND SCHEDULING   9
Parallel Computer models: The state of computing, Multiprocessors and Multicomputers, Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks.
Program and network properties: Conditions of parallelism, Program partitioning and scheduling, program flow mechanisms, System interconnect architectures.

UNIT II- SCALABLE PERFORMANCES & HARDWARE TECHNOLGIES   9
Principles of scalable performance: Performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.
Processor and memory hierarchy: Advanced processor technology, Superscalar and vector processors, memory hierarchy technology, virtual memory technology.

UNIT III- MEMORY ORGANIZATIONS & PIPELINING   9
Bus cache and shared memory: backplane bus systems, cache memory organizations,   shared memory organizations, sequential and weak consistency models.
Pipelining: Linear and non-Linear Pipeline processors-Instruction pipeline design and Arithmetic pipeline design.

UNIT IV- PARALLEL & SCALABLE ARCHITECTURES   9
Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V-SOFTWARE & PARALLEL PROCESSING   9
Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

<div align="right">**TOTAL: 45 HOURS**</div>

TEXT BOOKS:
1. Kai Hwang "Advanced Computer Architecture", Tata McGraw Hill International, 2001.

REFERENCE BOOKS:
1.John L. Hennessy, David A. Petterson, "Computer Architecture: A Quantitative Approach", 4th Edition, Elsevier, 2007.
2.Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced computer Architecture – A design Space Approach". Pearson Education,2003.

3.David E. Culler, Jaswinder Pal Singh with Anoop Gupta "Parallel Computer Architecture" ,Elsevier, 2004.
4.John P. Shen. "Modern processor design Fundamentals of super scalar processors", Tata McGraw Hill 2003.
5.Sajjan G. Shiva "Advanced Computer Architecture", Taylor & Francis, 2008.
6.V.Rajaraman, C.Siva Ram Murthy, "Parallel Computers- Architecture and Programming", Prentice Hall India, 2008.

	Semester III	L	T	P	C
	SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS	**3**	**1**	**0**	**4**

AIM:

To introduce some C concepts relavant to embedded systems with 80x86 family as basis and UML.

OBJECTIVE:

To make the student learn: use of C language for embedded applications, real time UML concepts, co-design methods.

UNIT I   LOW LEVEL PROGRAMMING IN C   9
Primitive data types – Functions – recursive functions – Pointers - Structures – Unions – Dynamic memory allocations – File handling – Linked lists

UNIT II   C AND ASSEMBLY   9
Programming in Assembly – Register usage conventions – typical use of addressing options – instruction sequencing – procedure call and return – parameter passing – retrieving parameters – everything in pass by value – temporary variables.

UNIT III   OBJECT-ORIENTED ANALYSIS AND DESIGN   9
Connecting the Object Model with the Use Case Model. Key Strategies for Object-Identification - Underline the Noun Strategy. Identify the Casual Objects - Identify Services (Passive Contributors) - Identify Real-World Items - Identify Physical Devices - Identify Key Concepts - Identify Transactions - Identify Persistent Information - Identify Visual Elements. Identify Control Elements - Apply Scenarios.

UNIT IV   UNIFIED MODELLING LANGUAGE   9
Object State Behaviour - UML State charts - Role of Scenarios in the Definition of Behaviour - Timing Diagrams - Sequence Diagrams - Event Hierarchies - Types and Strategies of Operations - Architectural Design in UML Concurrency Design - Representing Tasks - System Task Diagram - Concurrent State Diagrams - Threads. Mechanistic Design - Simple Patterns.

UNIT V   CASE STUDIES   9
Multi threaded applications – assembling embedded applications – polled waiting loop and interrupt driven I/O – preemptive kernels and shared resources - system timer – scheduling – client server computing.

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:
1. Bruce Powel Douglas, "Real-Time UML, Second Edition: Developing Efficient Objects for Embedded Systems (The Addison-Wesley Object Technology Series)", 2 edition (October 29, 1999), Addison-Wesley.
2. Hassan Gomma, "Designing Concurrent, Distributed, and Real-Time applications with UML.
3. Daniel W. Lewis, "Fundamentals of Embedded Software where C and Assembly meet" PHI 2002.

Semester III	L	T	P	C
VLSI ARCHITECTURE AND DESIGN METHODOLOGIES	3	1	0	4

AIM:

This course will introduce approaches and methodologies for VLSI architectures of signal processing.

OBJECTIVE:

- ➢ At the end of this course the student can have knowledge about the basic approaches and methodologies for VLSI architectures of signal processing.
- ➢ The students will also have hands-on VLSI system design experience using hardware description language (HDL) and commercial EDA tools (Synopsys).

UNIT I   INTRODUCTION   9

Overview of digital VLSI design methodologies - Trends in IC technology – advanced Boolean algebra - Shannon's expansion theorem - consensus theorem - Octal designation - Run measure - Buffer gates - Gate Expander - Reed Muller expansion - Synthesis of multiple output combinational logic circuits by product map method - Design of static hazard free and dynamic hazard free logic circuits.

UNIT II   ANALOG VLSI AND HIGH SPEED VLSI   9

Introduction to analog VLSI - Realisation of Neural networks and switched capacitor filters - sub-micron technology and GaAs VLSI technology.

UNIT III   PROGRAMMABLE ASICS   9

Anti fuse – static RAM – EPROM and EEPROM technology - PREP bench marks –Actel ACT - Xilinx LCA – Altera FLEX - Altera MAX DC & AC inputs and outputs-clock and power inputs - Xilinx I/O blocks.

UNIT IV   PROGRAMMABLE ASIC DESIGN SOFTWARE   9

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 - Altera MAX 9000 - Design systems – Logic synthesis – Half gate ASIC – schematic entry – Low level design language – PLA tools – EDIF – CFI design representation

UNIT V   LOGIC SYNTHESIS, SIMULATION AND TESTING   9

Basic features of VHDL language for behavioural modelling and simulation - Summary of VHDL data types – dataflow and structural modelling – VHDL and logic synthesis – types of simulation – boundary scan test-fault simulation – automatic test pattern generation

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

REFERENCES:

1. William I. Fletcher "An Engineering approach to Digital Design" Prentice Hall of India 1996
2. Amar Mukherjee, Introduction to NMOS and CMOS VLSI system design, Prentice hall 1986
3. M.J.S Smith "Application – specific integrates circuits", Addison Wesley Longman Inc.1997
4. Frederick J. Hill and Gerald R. Peterson, "Computer Aided Logical Design with emphasisonVLSI".

Semester IV	L	T	P	C
ADVANCED DIGITAL IMAGE PROCESSING	3	1	0	4

AIM:

This course aims to provide students with an understanding of digital image processing techniques, including image reconstruction and restoration, segmentation and enhancement, also colour and morphological image processing techniques.

OBJECTIVE:
Upon successful completion of this course, students should be able to understand all types of image processing techniques.

UNIT I: INTRODUCTION TO IMAGE PROCESSING SYSTEMS & IMAGETRANSFORMS
9

Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Applications of Digital image processing

Introduction, Need for transform, Image transforms, Fourier transform, 2 D Discrete Fourier transform and its transforms, Importance of phase, Walsh transform, Hadamard transform, Haar transform, slant transform Discrete cosine transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms.

UNIT II: IMAGE ENHANCEMENT & IMAGE RESTORATION   9

Introduction to image enhancement, Enhancement in spatial domain, enhancement through point operation, Types of point operation, Histogram manipulation, Linear Gray level transformation, Nonlinear Gray level transformation, Local or neighbourhood operation, Median filter, Image sharpening, Bit plane slicing, Image enhancement in the frequency domain.

Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution

UNIT III: IMAGE SEGMENTATION AND IMAGE COMPRESSION   9

Introduction to image segmentation, Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour

Introduction, Need for image compression, Redundancy in images, Classification of redundancy in images, image compression scheme, Classification of image compression schemes, Fundamentals of information theory, Run length coding, Shannon – Fano coding, Huffman coding, Arithmetic coding, Predictive coding, Transformed based compression, Image compression standard, Wavelet-based image compression

UNIT IV: COLOUR IMAGE PROCESSING   **9**

Introduction, Light and colour, colour formation, Human perception of colour, colour model The chromaticity diagram, colour image quatization, Histogram of colour image, colour image filtering, Gamma correction of a colour image, colour image segmentation.

UNIT V: MORPHOLOGICAL IMAGE PROCESSING   **9**

Preliminaries-Dilation & Erosion, Opening & Closing, Hit or Miss Transformation,Basic Morphological Algorithms,Extension to Gray scale Images.

<div align="right">

TUTORIAL: 15 HOURS

TOTAL: 60 HOURS

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REFERENCES:

1) S.Jayaraman, S.Esakkirajan and T.VeeraKumar, "Digital Image processing, Tata Mc Graw Hill publishers, 2009

2) Gonzalez, R.E.Woods, "Digital Image Processing", 3rd Edition, Pearson Education, India, 2009.

3) John W.Woods, "Multidimensional Signal, Image and Video Processing and Coding" Elsevier Academic Press Publications 2006, ISBN-13: 978-0-12– 088516-9.

Semester IV	L	T	P	C
EMBEDDED SYSTEMS LAB – II	0	0	2	2

1. ATMEL CPLDs – Prochip designer

a) Schematic entry

b) VHDL entry

2. AT40K FPGA series – synthesis – design – simulation of application programs

3. Xilinx EDA design tools – device programming –PROM programming

4. ALTERA and Mentor graphics – IC design tools

5. Code compressor studio for embedded DSP using Texas tool kit

6. Cell based ASICs – sample programs for risk and security plans

7. IPCORE usage in VOIP through SoC2 tools

8. FPSLIC synthesis testing and examples

9. Third party tools for embedded java and embedded C++ applications through cadence tools.

TOTAL: 30 HOURS

ELECTIVE	L	T	P	C
ASIC DESIGN	3	0	0	3

AIM:

As VLSI implementation is largely in ASIC, this subject is introduced here.

OBJECTIVE:

To make the student learn the fundamentals of ASIC and its design methods.

UNIT I   INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN
                                                                                                9
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture

UNIT II   PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS PROGRAMMABLE ASIC I/O CELLS   9
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III   PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC   DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY   9
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV   LOGIC SYNTHESIS, SIMULATION AND TESTING   9
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V   ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING
                                                                                                9
System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL: 45 HOURS

REFERENCES:

1. M.J.S .Smith, "Application - Specific Integrated Circuits "- Addison -Wesley Longman Inc., 1997.
2. Andrew Brown, " VLSI Circuits and Systems in Silicon", McGraw Hill, 1991
3. S.D. Brown, R.J. Francis, J. Rox, Z.G. Uranesic, " Field Programmable Gate Arrays ", Kluwer Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing ", Mc Graw Hill, 1994.
5. S. Y. Kung, H. J. Whilo House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
6. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

	ELECTIVE	L	T	P	C
	ADVANCED ROBOTICS & AUTOMATION	**3**	**0**	**0**	**3**

AIM:
      The aim of this course is to develop and deploy advances in measurement science to safely increase the versatility, autonomy, and rapid re-tasking of intelligent robots and automation technologies.

OBJECTIVE:
      At the end of this course student will infer some knowledge regarding advanced robotics and automation.

UNIT I INTRODUCTION   **9**
Geometric configuration of robots - manipulators - drive systems - internal and external sensors - end effectors - control systems - robot programming languages and applications - Introduction to robotic vision.

UNIT II ROBOT ARM KINEMATICS   **9**
Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation - Denavit Hattenberg representation and various arm configurations.

UNIT III ROBOT ARM DYNAMICS   **9**
Lagrange - Euler formulation, joint velocities - kinetic energy - potential energy and motion equations – generalized D'Alembert equations of motion.

UNIT IV ROBOT APPLICATONS   **9**
Material Transfer & Machine Loading / Unloading General Consideration in robot material handling transfer applications – Machine loading and unloading. Processing Operations Spot welding – Continuous arc welding - spray coating – other processing operations using robots.

UNIT V ASSEMBLY AND INSPECTION   **9**
Assembly and robotic assembly automation – Parts presentation methods – assembly operation – Compliance and the Remote Center Compliance(RCC) device – Assembly system Configurations – Adaptable, Programmable assembly system – Designing for robotic assembly – Inspection automation.
                                 TOTAL: 45 HOURS

REFERENCES:
1. Fu, Gonazlez.K.S., R.C. and Lee, C.S.G., Robotics (Control, Sensing, Vision and Intelligence), McGraw Hill, 1968
2. Wesley.E, Snyder.R, Industrial Robots, "Computer Interfacing and Control", Prentice Hall International Edition, 1988
3. Asada and Slotine, "Robot analysis and Control", John Wiley and sons, 1986
4. Philippe Coiffet, "Robot technology" - Vol.II (Modelling and Control), Prentice Hall Inc., 1983
5. Groover.M.P., Mitchell, Weiss, "Industrial Robotics Technology Programming and Applications", Tata McGraw Hill, 1986

ELECTIVE	L	T	P	C
VIDE PROCESSING	**3**	**0**	**0**	**3**

AIM

The purpose of Video Processing course is to cover the fundamentals of digital video signal generation and further processing over the communication systems.

OBJECTIVE

To learn the basic concepts of video processing
To learn about the various methodologies for motion estimation
To learn the basic concepts of coding systems
To understand about the waveform based video coding techniques
To understand about the content dependent and scalable video coding techniques

UNIT I VIDEO FORMATION, PERCEPTION AND REPRESENTATION   9

Color Perception and Specification, Video Capture and Display, Analog Video Raster, Analog Color Television Systems, Digital Video.

UNIT II TWO-DIMENSIONAL MOTION ESTIMATION   9

General Methodologies, Pixel-Based Motion Estimation,, Block Matching Algorithm, Mesh-based Motion estimation, Global Motion Estimation, Region –Based Motion Estimation, Mutiresolution Motion Estimation, Application of Motion Estimation in Video Coding. Feature-based Motion Estimation.

UNIT III FOUNDATONS OF VIDEO CODING   9

Overview of Coding Systems, Basic Notions in Probability and Information Theory, Information Theory for Source Coding, Binary Encoding, Scalar Quantization , Vector Quantization.

UNIT IV WAVEFORM-BASED VIDEO CODING   9

Block-Based Transform Coding, Predictive Coding, Video Coding Using Temporal Prediction and Transform Coding.

UNIT V CONTENT-DEPENDENT & SCALABLE VIDEO CODING   9

Two-Dimensional Shape Coding, Texture coding for Arbitrarily Shaped Regions, Joint Shape & Texture Coding, Region-Based Video Coding, Object-based Video Coding. Basic Modes of Scalability,Object Based Scalability, Wavelet-transform Based Coding.

TOTAL HOURS: 45

TEXT BOOKS:
1. YaoWang, Jorn Ostermann, Ya-Qin Zhang,"Video Processing & Communication", Pearson Education - India, New Delhi, Prentice Hall, 2002.

REFERENCES:
1. M. Tekalp, Digital Video Processing, Prentice Hall, 1995.

ELECTIVE	L	T	P	C
RELIABILITY ENGINEERING FOR ELECTRONICS	3	0	0	3

AIM:
　　　This course aims to provide the student to apply engineering knowledge and specialist techniques to prevent or to reduce the likelihood or frequency of failures.

OBJECTIVE:
　　　The students will be able to understand the ways in which product fail, the effects of failure and aspects of design, manufacture, maintenance and use which affect the likelihood of failure.

UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE 9
Statistical distribution, statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference, Safety margin and loading roughness on reliability.

UNIT II RELIABILITY PREDICTION, MODELLING AND DESIGN   9
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY   9
Reliablity of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design, software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS   9
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MANAGEMENT   9
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for
reliability.
　　　　　　　　　　　　　　　　　　　　　　　　TOTAL: 45 HOURS

REFERENCES:
1. Patrick D.T. O'Connor, David Newton and Richard Bromley, "Practical Reliability Engineering", 4th edition, John Wiley & Sons, 2002
2. David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, "AT & T Reliability Manual", 5th Edition, New

York, 1998

3. Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, New York, 2000

4. Lewis, "Introduction to Reliability Engineering", 2nd Edition, Wiley International, 1996

	ELECTIVE	L	T	P	C
	ELECTROMAGNETIC INTERFERENCE & COMPATIBILITY	3	0	0	3

AIM:

To understand different electromagnetic Interference problems occurring in Intersystem and in inter system and their possible mitigation techniques in Electronic design.

OBJECTIVES:
- To understand EMI Sources, EMI problems and their solution methods in PCB level / Subsystem and system level design.

- To measure the emission immunity level from different systems to couple with the prescribed EMC standards.

UNIT I EMI/EMC CONCEPTS   **9**
EMI- EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES   **9**
Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling; Differential mode coupling ; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES   **9**
Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

UNIT IV EMC DESIGN OF PCBS   **9**
Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS   **9**
Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

                                                                TOTAL: 45 HOURS

REFERENCES:

1.V.P.Kodali, "Engineering EMC Principles, Measurements and Technologies", IEEE Press, Newyork, 1996.
2.Henry W.Ott.,"Noise Reduction Techniques in Electronic Systems", A Wiley Inter Science Publications, John Wiley and Sons, Newyork, 1988.
3.Bemhard Keiser, "Principles of Electromagnetic Compatibility", 3rd Ed, Artech house, Norwood, 1986.
4.C.R.Paul,"Introduction to Electromagnetic Compatibility" , John Wiley and Sons,   Inc, 1992.
5.Don R.J.White Consultant Incorporate, "Handbook of EMI/EMC" , Vol I-V, 1988.

ELECTIVE	L	T	P	C
VLSI SIGNAL PROCESSING	**3**	**0**	**0**	**3**

AIM:

      To expose students to the advanced digital signal processing systems for VLSI and associated EDA Tools.

OBJECTIVE:

      At the end of this course the student will be able knowing methods and techniques for implementation of DSP systems.

UNIT I   INTRODUCTION TO DSP SYSTEMS   9
Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II   RETIMING   9
Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT III   FAST CONVOLUTION   9
Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm; Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition, Clustered Look-Ahead pipelining, parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters, relaxed look-ahead, pipelined LMS adaptive filter.

UNIT IV   BIT-LEVEL ARITHMETIC ARCHITECTURES   9
Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement.

UNIT V   PROGRAMMING DIGITAL SIGNAL PROCESSORS   9
Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low

power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

TOTAL: 45 HOURS

REFERENCES:
1. Keshab K.Parhi, " VLSI Digital Signal Processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Gary Yeap, 'Practical Low Power Digital VLSI Design,' Kluwer Academic Publishers, 1998.
3. Mohammed Ismail and Terri Fiez, " Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
4. S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

ELECTIVE	L	T	P	C
CYBER SECURITY	3	0	0	3

AIM

To produce the knowledge on cyber security essentials

OBJECTIVE

- To study the cyber security fundamentals
- To study the various techniques on attack and exploitation
- To study in detail about malicious code
- To study about defense and analysis techniques

UNIT I CYBER SECURITY FUNDAMENTALS

Network and security concepts – basic cryptography – Symmetric encryption – Public key Encryption – DNS – Firewalls – Virtualization – Radio Frequency Identification – Microsoft Windows security Principles.

UNIT II ATTACKER TECHNIQUES AND MOTIVATIONS

Antiforensics – Tunneling techniques – Fraud Techniques - Threat Infrastructure.

UNIT III EXPLOITATION

Techniques to gain a foot hold – Misdirection, Reconnaissance, and disruption methods.

UNIT IV MALICIOUS CODE

Self Replication Malicious code – Evading Detection and Elevating privileges – Stealing Information and Exploitation.

UNIT V DEFENSE AND ANALYSIS TECHNIQUES

Memory Forensics – Honeypots – Malicious code naming – Automated malicious code analysis systems – Intrusion detection systems – Defense special file investigation tools.

TOTAL HOURS: 45

TEXT BOOK

1. James Graham, Richard Howard and Ryan Olson, "Cyber Security Essentials", CRC Press, Taylor & Francis Group, 2011.

REFERENCE BOOKS

1. By Dan Shoemaker, Ph.D., William Arthur Conklin, Wm Arthur Conklin, "Cybersecurity: The Essential Body of Knowledge**",** Cengage Learning, 2012.
2. Ali Jahangiri, "Live Hacking: The Ultimate Guide to hacking Techniques & Counter measures for Ethical Hackers & IT Security Experts", 2009.

	ELECTIVE	L	T	P	C
	INTERNETWORKING MULTIMEDIA	**3**	**0**	**0**	**3**

AIM:
　　　　Main aim of this course is to make the students understand in identifying and analyzing the requirements that a distributed multimedia application may enforce on the communication network.

OBJECTIVE:
　　　　At the end of this course students have knowledge in distributing multimedia application over the communication network.

UNIT I MULTIMEDIA NETWORKING　　　　　　　　　　9
Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video.

UNIT II BROAD BAND NETWORK TECHNOLOGY　　　　9
Broadband services, ATM and IP , IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance.

UNIT III MULTICAST AND TRANSPORT PROTOCOL　　　9
Multicast over shared media network, multicast routing and addressing, scaping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP.

UNIT IV MEDIA - ON – DEMAND　　　　　　　　　　9
Storage and media servers, voice and video over IP, MPEG over ATM/IP, indexing synchronization of requests, recording and remote control.

UNIT V APPLICATIONS　　　　　　　　　　　　　　9
MIME, Peer-to-peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy.
**　　　　　　　　　　　　　　　　　　　　　　TOTAL HOURS: 45**

REFERENCES:
1. Jon Crowcroft, Mark Handley, Ian Wakeman. Internetworking Multimedia, Harcourt Asia Pvt.Ltd. Singapore, 1998.
2. B.O. Szuprowicz, Multimedia Networking, McGraw Hill, NewYork. 1995
3. Tay Vaughan, Multimedia making it to work, 4ed,Tata McGrawHill, NewDelhi,2000.

	ELECTIVE	L	T	P	C
	ANALOG VLSI DESIGN	3	0	0	3

AIM:

This course is intended to introduce the student to learn about Device Modeling- Various types of analog systems- CMOS amplifiers and Comparators.

OBJECTIVE:

By the end of the term, students should be able to:

➢ Demonstrate an understanding of MOS terminal characteristics and capacitive effects.

➢ Create integrated circuit layouts showing an awareness of the underlying process technology and layout parasitic as well as their impact on circuit performance.

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGESIGNAL PROCESSING   9

Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOSTransistor-Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING   9

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched -Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks -Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS   9

First-order and Second SC Circuits-Bilinear Transformation -Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter-Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit igma-Delta Modulators-Interpolative Modulators – Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS
9

Fault modelling and Simulation -Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test uses-Design for Electron - Beam Testablity-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT   9
Review of Statistical Concepts -Statistical Device Modeling-Statistical Circuit Simulation- Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout- Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL: 45 HOURS

REFERENCES:
1. Mohammed Ismail, Terri Fief, "Analog VLSI signal and Information Processing ", McGraw-Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May,"Analog VLSI Design -NMOS and CMOS ", Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994

ELECTIVE	L	T	P	C
LOW POWER VLSI DESIGN	**3**	**0**	**0**	**3**

AIM:

As there is always a need for power efficient circuits and devices, this course explain the methods for low power VLSI design.

OBJECTIVE:

At the end of this course the student will be able to design Low power CMOS designs, for digital circuits.

UNIT I 9

Introduction - Simulation - Power Analysis-Probabilistic Power Analysis.

UNIT II 9

Circuit -Logic - Special Techniques - Architecture and Systems.

UNIT III 9

Advanced Techniques - Low Power CMOS VLSI Design - Physics of Power Dissipation in CMOS FET Devices.

UNIT IV 9

Power Estimation - Synthesis for Low Power - Design and Test of Low Voltages - CMOS Circuits.

UNIT V 9

Low Power Static RAM Architectures -Low Energy Computing Using Energy Recovery Techniques - Software Design for Low Power.

TOTAL: 45 HOURS

REFERENCES:

1. Gary Yeap " Practical Low Power Digital VLSI Design",1997.
2. Kaushik Roy, Sharat Prasad, "Low Power CMOS VLSI Circuit Design", 2000.

ELECTIVE	L	T	P	C
EMBEDDED LINUX	3	0	0	3

AIM:

To provide knowledge on basic embedded drivers, embedded Linux and their functioning.

OBJECTIVE:

To study embedded linux and their device drivers functioning and applications.

UNIT I FUNDAMENTALS OF OPERATING SYSTEMS   9
Overview of operating systems – Process and threads – Processes and Programs – Programmer view of processes – OS View of processes – Threads - Scheduling – Non preemptive and preemptive scheduling – Real Time Scheduling – Process Synchronization – Semaphores – Message Passing – Mailboxes – Deadlocks – Synchronization and scheduling in multiprocessor Operating Systems

UNIT II   LINUX FUNDAMENTALS   9
Introduction to Linux – Basic Linux commands and concepts – Logging in - Shells -   Basic text editing - Advanced shells and shell scripting – Linux File System –Linux programming - Processes and threads in Linux - Inter process communication – Devices – Linux System calls

UNIT III   INTRODUCTION TO EMBEDDED LINUX   9
Embedded Linux – Introduction – Advantages- Embedded Linux Distributions - Architecture - Linux kernel architecture - User space – linux startup sequence - GNU cross platform Tool chain

UNIT IV   BOARD SUPPORT PACKAGE AND EMBEDDED STORAGE   9
Inclusion of BSP in kernel build procedure - The bootloader Interface – Memory Map – Interrupt Management – PCI Subsystem – Timers – UART – Power Management – Embedded Storage – Flash Map – Memory Technology Device (MTD) –MTD Architecture - MTD Driver for NOR Flash – The Flash Mapping drivers – MTD Block and character devices – mtdutils package – Embedded File Systems – Optimizing storage space – Turning kernel memory

UNIT V   EMBEDDED DRIVERS AND APPLICATION PORTING   9
Linux serial driver – Ethernet driver – I2C subsystem – USB gadgets – Watchdog timer – Kernel Modules – Application porting roadmap - Programming with pthreads – Operting System Porting Layer – Kernel API Driver - Case studies - RT Linux – uClinux

TOTAL: 45 HOURS

REFERENCE BOOKS

1. Dhananjay M. Dhamdhere, 'Operating Systems A concept based Approach', Tata Mcgraw-Hill Publishing Company Ltd
2. Matthias Kalle Dalheimer, Matt Welsh, 'Running Linux', O'Reilly Publications 2005
3. Mark Mitchell, Jeffrey Oldham and Alex Samuel 'Advanced Linux Programming' New Riders Publications
4. P. Raghavan ,Amol Lad , Sriram Neelakandan, 'Embedded Linux System Design and Development', Auerbach Publications 2006 Karim Yaghmour, 'Building Embedded Linux Systems', O'Reilly Publications 2003

	ELECTIVE	L	T	P	C
	MOBILE COMPUTING	3	0	0	3

AIM:

The aim of this course is provide an introduction of an advanced element of learning in the field of wireless communication and also expose the students to the concepts of wireless devices and mobile computing.

OBJECTIVE:

At the end of this course the student should be able to understand the concept of mobile computing and architecture of mobile communication.

UNIT I INTRODUCTION   9

Basics of mobile computing - Medium access control – Telecommunication systems – Satellite systems – Broadcast systems.

UNIT II   STANDARDS   9

Wireless LAN – IEEE 802.11 – Frequency Hopping spread spectrum – Direct sequence and spread spectrum - HIPERLAN – Bluetooth.

UNIT III   ADHOC NETWORKS   9

Characteristics – Performance issues – Routing in mobile hosts – Destination sequence distance vector – Dynamic source routing – Hierarchical Algorithms.

UNIT IV   NETWORK ISSUES   9

Mobile IP – DHCP – Mobile transport layer – Indirect TCP – Snooping TCP – Transmission / time-out freezing – Selective retransmission – Transaction oriented TCP.

UNIT V   APPLICATION ISSUES   9

Wireless application protocol – Dynamic DNS - File systems – Synchronization protocol – Context-aware applications – Security – Analysis of existing wireless network.

TOTAL: 45 HOURS

REFERENCES:

1. J. Schiller, Mobile Communications, Addison Wesley, 2000.
2. William C.Y.Lee, Mobile Communication Design Fundamentals, John Wiley, 1993.

ELECTIVE	L	T	P	C
REAL TIME SYSTEMS	3	0	0	3

AIM:

Since the concepts of real time systems and their analysis is very essential for embedded students this subject is given.

OBJECTIVE:

To make the student learn, all real time aspects of various system components, like OS, memory, communication and an introduction to reliability evaluation methods.

UNIT I   INTRODUCTION   9

Introduction - issues in real time computing - structure of a real time system - task classes - performance measures for real time systems - estimating program run times - task assignment and scheduling - classical uniprocessor scheduling algorithms - uniprocessor scheduling of IRIS tasks - tasks assignment - mode changes - fault tolerant scheduling.

UNIT II   PROGRAMMING LANGUAGES AND TOOLS   9

Language features - desired language characteristics - data typing - control structures - facilitating hierarchical decomposition - package - run-time error handling - overloading and generics - multitasking - low level programming - task scheduling - timing specifications - programming environments - run-time support – code generation.

UNIT III   REAL TIME DATABASES   9

Real time database - basic definition - real time Vs general-purpose database - main memory databases - transaction priorities - transaction aborts - concurrency control issues - disk scheduling algorithms - two-phase approach to improve predictability - maintaining serialization consistency - databases for hard real time systems.

UNIT IV   COMMUNICATION   9

Real time communication - communications media - network topologies - protocols – buffering data – synchronization – dead lock – mail boxes and semaphores - fault tolerance techniques - fault types - fault detection - fault error containment - redundancy -data diversity - reversal checks - integrated handling.

UNIT V   EVALUATION TECHNIQUES   9

Reliability evaluation techniques - reliability models for hardware redundancy - software error models – response time calculation – interrupt latency – time loading and its measurement – reducing response times – analysis of memory requirements – reducing memory loading

TOTAL: 45 HOURS

TEXT BOOK:

1. C.M.Krishna, Kang G. Shin, Real - Time Systems, McGraw-Hill International Editions, 2008.

REFERENCES:

1. Stuart Bennett, Real Time Computer Control -An Introduction, PHI, 1988.

2. Peter D Lawrence, Real Time Micro Computer System Design -An Introduction, McGraw-Hill, 1988.

3. S.T.Allworth and R.N.Zobel, Introduction to real time software design, Macmillan, II Edition, 1987.

4. Real time systems design and analysis - An Engineers handbook 2nd edition - phillip A.Laplante, IEEE Press, IEEE Computer Society Press, 2001

ELECTIVE	L	T	P	C
EMBEDDED PROCESSORS	**3**	**0**	**0**	**3**

AIM:

To enhance the knowledge of the student about basic embedded architectures and their applications of high end processors.

OBJECTIVE:
- To study basic processor accessories.
- To study DSP & ARM Processors and their applications.

UNIT I INTRODUCTION 9

Introduction to Processor and peripherals – keyboards – Multiplexed LED Displays –Character LCD modules –Time of Day Clock – Timer Manager – Discrete Inputs and Outputs – Fixed point Math – Analog Math.

UNIT II ANALOG DSP 9

Analog DSP "Blackfin" Processor – introduction, architecture, features, applications -instruction-set architecture and hardware micro architecture – ADSP 2100 – introduction, architecture, features, applications.

UNIT III ARM PROCESSOR 9

Introduction, architecture, instruction set, addressing modes, applications – Palm One OS5-based device with ARM processor – ARM application processor – ARM720T and ARM920T.

UNIT IV OPEN MULTIMEDIA APPLICATION PLATFORM 9

Introduction, architecture, instruction set, addressing modes, applications – OMAP5910 –module overview, display specification, LCD controller operation, Lookup palette, color dithering, output FIFO, LCD controller pins, LCD controller registers, interface to LCD panel signal reset values.

UNIT V CASE STUDY 9

Audio/video and VOIP application for multimedia application using OMAP TI-5012 – TI OMAP Applications Processor - OMAP2420 and OMAP1710 – architecture, features and applications.

TOTAL: 45 HOURS

TEXT BOOK:
1. Jean J Labrose, "Embedded Systems Building Blocks", CMP Books, second edition,2005.
REFERENCE BOOKS:
1. ARM reference manual from Texas Instruments, 2006.
2. OMAP reference manual from Texas Instruments, 2006.
3. Technical documents from Texas Instruments Hall for OMAP TI – 5012, 2006.

ELECTIVE	L	T	P	C
MIXED SIGNAL SYSTEM	3	0	0	3

AIM:
      This course aims to make student understand basic current mixed signal systems, circuit building blocks, basic operation method and design method.

OBJECTIVE:
      At the end of the course the students will be provided with unified view of physical system architectures from chip, circuit board, to cabinets. They will also have knowledge on basic theory and analysis methods as well as design practice for high performance interconnections and packaging in such complex, mixed-signal end-products as mobile terminals and base-stations.

UNIT I INTRODUCTION TO ANALOG AND MIXED SIGNAL CIRCUITS   9
Design & Verification – Applications Challenges - Market Perspective - Analog CMOS circuits - Current Mirrors - Current and Voltage References - Bandgap References.

UNIT II CMOS AMPLIFIERS   9
Opamps - High Performance CMOS amplifiers – Comparators – Characterization - Two stage open loop comparators - Discrete time comparators - High-speed comparators.

UNIT III SWITCHED CAPACITOR CIRCUITS   9
Switched Capacitor (SC) Introduction - offset cancellation - clock feed - through - Switched Capacitor amplifiers - Switched Capacitor Integrators - Switched Capacitor filters.

UNIT IV DATA CONVERTERS   9
Introduction - Nyquist rate converters – Over sampling converters - Pipelined/parallel converters - High speed ADC design, High speed DAC design and Mixed signal design for radar application - ADC and DAC modules used for LIGO.

UNIT V PHASE LOCKED LOOPS   9
Introduction - Frequency Synthesizers - Design of PLL and Frequency Synthesizers –PLL with voltage driven oscillator – PLL with current driven oscillator – ETPLL – PLL synthesizer oscillator by MC14046B.

TOTAL: 45 HOURS

TEXT BOOKS:
1. Allen, "CMOS Analog Circuit Design", Oxford, 2005.
2. Behzad Razavi, "Design of Analog CMOS integrated circuit", Tata Mc Graw Hill,2004.

REFERENCE BOOKS:
1. Breems, "Continuous-Time Sigma Delta Modulations for A/D Conversion",Kluwer,2002.
2. Michelle Steyaert, "Analog Circuit Design", Kluwer, 2003.
3. Gray & Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 2004.
4. Jacob Baker, "CMOS Mixed-Signal Circuit Design", Wiley, 2004.
5. Behzad Razavi, "Design of Analog CMOS Integrated Circuit", Tata Mc Graw Hill, 2004.

	ELECTIVE	L	T	P	C
	EMBEDDED CONTROL SYSTEMS	3	0	0	3

AIM:
To introduce the basic concepts of control systems and its embedded implementation.

OBJECTIVE:
To make the student learn, basics of control systems, application methods of control theory in embedded systems.

UNIT I INTRODUCTION 9
Controlling the hardware with software – data lines – numbering systems – address lines - ports – schematic representation – bit masking – programmable peripheral interface – switch input detection.

UNIT II INPUT-OUTPUT DEVICES 9
Keyboard basics – keyboard scanning algorithm – Multiplexed LED displays – character LCD modules – LCD module display – configuration – Time-of-day clock – Timer manager - interrupts - interrupt service routines – IRQ - ISR - interrupt vector or dispatch table multiple-point - interrupt-driven pulse width modulation.

UNIT III D/A AND A/D CONVERSION 9
R 2R ladder - more on Op-Amps - virtual ground - resistor network analysis - port offsets - triangle waves analog vs digital values - ADC0809 – comparator - successive approximation - the ADC clock - ripple counter - D flip-flop - Q and NOT Q - aliasing – multiplexer - Auto port detect - recording and playing back voice - capturing analog information in the timer interrupt service routine - automatic, multiple channel analog to digital data acquisition.

UNIT IV ASYNCHRONOUS SERIAL COMMUNICATION 9
Asynchronous serial communication – RS-232 – RS-485 – sending and receiving data – serial ports on PC – low-level PC serial I/O module - buffered serial I/O.

UNIT V CASE STUDIES 9
Multiple closure problems – basic outputs with PPI – controlling motors – bidirectional control of motors – H bridge – Telephonic systems – burglar alarms – fire alarms – inventory control systems.
TOTAL: 45 HOURS

REFERENCES:

1. Jean J. Labrosse, "Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C", The publisher, Paul Temme, 1999.
2. Ball S.R., Embedded microprocessor Systems – Real World Design, Prentice Hall, 1996.

ELECTIVE	L	T	P	C
MEMS	**3**	**0**	**0**	**3**

3. Herma K, " Real Time Systems – Design for distributed Embedded Applications", Kluwer Academic, 1997

4. Daniel W. Lewis, "Fundamentals of Embedded Software where C and Assembly meet"PHI2002.

AIM:

This course is an introduction to MEMS, which also uses micro electronics. This course fulfills the need of electronic engineer who want to create MEMS devices.

OBJECTIVE:

At the end of this course, the student will have knowledge on MEMS materials, fabrication and micro sensor design.

UNIT I INTRODUCTION 9

MEMS-Micro fabrications for MEMS -Surface micromachining of silicon -Wafer bonding for MEMS- LIGA process-Micromachining of polymeric MEMS devices -Three-dimensional microfabrications.Materials: Materials for MEMS - Metal and metal alloys for MEMS - Polymers for MEMS - Other materials for MEMS.Metals : Evaporation –Sputtering.Semiconductors :Electrical and chemical properties-Growth and deposition.Thin films for MEMS and their deposition techniques -Oxide film formation by thermal --oxidation -Deposition of silicon dioxide and silicon nitride -Polysilicon film deposition -Ferroelectric thin films. Materials for polymer MEMS :Classification of polymers -UV radiation curing -SU-8 for polymer MEMS.

UNIT II MICROSENSING FOR MEMS 9

Piezoresistive sensing - Capacitive sensing - Piezoelectric sensing - Resonant sensing - Surface acoustic wave sensors.Transducers: *E*lectromechanical transducers-Piezoelectric transducers -Electrostrictive transducers-Magnetostrictive transducers -Electrostatic actuators-Electromagnetic transducers - Electrodynamic transducers- Actuators: Electrothermal actuators-Comparison of electromechanical actuation schemes.

UNIT III MICRO MACHINING 9

Micromachning : Bulk micromachining for silicon-based MEMS -Isotropic and orientation-dependent wet etching- Dry etching -Buried oxide process -Silicon fusion bonding -Anodic bonding -Silicon surface micromachining Sacrificial layer technology - Material systems in sacrificial layer technology - Surface micromachining using plasma etching-Combined integrated-circuit technology and anisotropic wet etching.

UNIT IV LITHOGRAPHY 9

Microstereolithography for polymer MEMS -Scanning method -Two-photon microstereolithography Surface micromachining of polymer MEMS -Projection method -Polymeric MEMS architecture with silicon, metal and ceramics-Microstereolithography integrated with thick film lithography.

UNIT V APPLICATIONS 9

Switching: Introduction- Switch parameters- Basics of switching - Mechanical switches-Electronic switches-Switches for RF and microwave applications - Mechanical RF switches - PIN diode RF switches

- Metal oxide semiconductor field effect transistors and monolithic microwave integrated circuits. RF MEMS switches: Integration and biasing issues for RF switches -Actuation mechanisms for MEMS devices-Electrostatic switching - Approaches for low-actuation-voltage switches - Mercury contact switches –Magnetic switching - Electromagnetic switching - Thermal switching. Dynamics of the switch operation: Switching time and dynamic response - Threshold voltage. MEMS switch design, modeling and evaluation: Electromechanical finite element analysis- RF design - MEMS switch design considerations.

TEXT BOOK:
1. Vijay K.Varadan, K.J.Vinoy and K.A.Jose, "RF MEMS and Their Applications(ISBN 0-470-84308-X)", 1st edition, John Wiley & Sons Ltd., West Sussex, England, 2003.

TOTAL: 45 HOURS

REFERENCE BOOKS :

1. P. Rai-choudhury, "MEMS and MOEMS Technology and Applications", 1st Edition PHI, 2009.
2. S. Senturia, Microsystem Design, Kluwer, 2001.
3. J.W. Gardner, V.K. Varadan, O.O. Awadelkarim, Microsensors, MEMS & Smart Devices John Wiley, 2001.
4. S. Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford Univ. Press, 2001
5. N Maluf An Introduction to Microelectromechanical Systems Engineering, Artech House

ELECTIVE	L	T	P	C
SOFT COMPUTING TECHNIQUES	3	0	0	3

AIM:

This course will provide a comprehensive and structured exposure to Soft Computing Techniques i.e Artificial Neural Networks, Fuzzy Logic, Genetic Algorithm, Particle Swarm Optimization.

OBJECTIVE:

To make the student learn, all types of soft computing techniques and how it is applied in various fields.

UNIT I INTRODUCTION   9

Approaches to intelligent control. Architecture for intelligent control. Symbolic reasoning system, rule-based systems, the AI approach. Knowledge representation. Expert systems.

UNIT II   ARTIFICIAL NEURAL NETWORKS   9

Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron. Learning and Training the neural network. Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations. Hopfield network, Self-organizing network and Recurrent network. Neural Network based controller

UNIT III   FUZZY LOGIC SYSTEM   9

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning. Introduction to fuzzy logic modeling and control. Fuzzification, inferencing and defuzzification. Fuzzy knowledge and rule bases. Fuzzy modeling and control schemes for nonlinear systems. Self-organizing fuzzy logic control. Fuzzy logic control for nonlinear time-delay system.

UNIT IV   GENETIC ALGORITHM   9

Basic concept of Genetic algorithm and detail algorithmic steps, adjustment of free parameters. Solution of typical control problems using genetic algorithm. Concept on some other search techniques like tabu search and anD-colony search techniques for solving optimization problems.

UNIT V   APPLICATIONS   9

GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using Matlab-Neural Network toolbox.
Stability analysis of Neural-Network interconnection systems. Implementation of fuzzy logic controller using Matlab fuzzy-logic toolbox. Stability analysis of fuzzy control systems.

                                TOTAL: 45 HOURS

REFERENCES
1. Jacek.M.Zurada, "Introduction to Artificial Neural Systems", Jaico Publishing   House, 1999.
2. Kosko,B. "Neural Networks And Fuzzy Systems", Prentice-Hall of India Pvt. Ltd., 1994.
3. Klir G.J. & Folger T.A. "Fuzzy sets, uncertainty and Information", Prentice-Hall of India Pvt. Ltd., 1993.
4. Zimmerman H.J. "Fuzzy set theory-and its Applications"-Kluwer Academic Publishers, 1994.
5. Driankov, Hellendroon, "Introduction to Fuzzy Control", Narosa Publishers.

ELECTIVE	L	T	P	C
DSP PROCESSORS	3	0	0	3

AIM:

The aim of the course is to teach students to use digital signal processors such as the TMS320C6xxx to perform real-time DSP on real signals.

OBJECTIVE:

This course brings together some of the theory and understanding you have gained in several other lecture courses and lets you apply that theory in solving the type of problem which might be encountered by a DSP engineer in industry.

UNIT I: FUNDAMENTALS OF PROGRAMMABLE DSP'S   9

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in P-DSP's – Multiple access memory – Multi – port memory – VLIW architecture – pipelining – Special Addressing modes in P-DSP's – On Chip Peripherals.

UNIT II: TMS320C5X PROCESSOR   9

Architecture – Assembly Language syntax- Addressing modes- Assembly language Instructions – pipeline structure, Operation – Block diagram of DSP Starter kit – Application Programs for processing real time signals.

UNIT III: TMS320C3X PROCESSOR   9

Architecture –Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation – Block diagram of DSP starter kit – Application, Programs for processing real time systems – Generating and finding the sum of series, Convolution of two sequences , Filter design.

UNIT IV: ADSP PROCESSORS   9

Architecture of ADSP-21XX and ADSP – 210XX series of DSP processors – Addressing modes and Assembly language instructions – Applications programs – Filter design, FFT calculation- Blackfin DSP Processor

UNIT V: ADVANCED PROCESSORS   9

Architecture of TMS320C54X: Pipe line operation, Code Composer Studio – Architecture of TMS320C6X – Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

TOTAL: 45 HOURS

TEXT BOOK:

1. B.Venkataramani and M.Bhaskar, "Digital Signal Processors – Architecture Programming and Application" - Tata McGraw – Hill Publishing Company Limited. New Delhi, 2008.

REFERENCES:

1. User guides Texas Instrumentation, Analog Devices, Motorola.

2. Simon Haykin "Adaptive filter theory", Prentice Hall, 2001.

3. Anil K Jain "Fundamental of Digtal image processing", Prentice Hall, 1989.

	ELECTIVE	L	T	P	C
	FUZZY LOGIC & ARTIFICIAL INTELLIGENCE	**3**	**0**	**0**	**3**

AIM:

This course aims to provide in depth knowledge to students about the artificial neural networks and also Fuzzy Logic as well as application of it.

OBJECTIVE:
- ➢ To make the student learn to improve their skills over artificial neural network and their application.
- ➢ To make the student learn to understand the concepts of fuzzy logic and their application.

UNIT I FUNDAMENTALS OF ANN   **9**

Introduction – Neuron Physiology – Specification of the brain – Eye neuron model - Fundamentals of ANN –Biological neurons and their artificial models – Learning processes –different learning rules – types of activation functions– training of ANN – Perceptron model (both single & multi layer) – training algorithm – problems solving using learning rules and algorithms – Linear seperability limitation and its over comings

UNIT II ANN ALGORITHM   **9**

Back propagation training algorithm – Counter propagation network – structure & operation – training – applications of BPN & CPN -Statistical method – Boltzmann training – Cauchy training – Hop field network and Boltzmann machine – Travelling sales man problem - BAM – Structure – types – encoding and retrieving – Adaptive resonance theory – Introduction to optical neural network – Cognitron & Neocognitron

UNIT III APPLICATION OF ANN   **9**

Hand written and character recognition – Visual Image recognition –- Communication systems – call processing– Switching – Traffic control – routing and scheduling –Articulation Controller - Neural Acceleration Chip (NAC)

UNIT IV INTRODUCTION TO FUZZY LOGIC   **9**

Introduction to fuzzy set theory — membership function - basic concepts of fuzzy sets – Operations on fuzzy sets and relations, classical set Vs fuzzy set – properties of fuzzy set – fuzzy logic control principles – fuzzy relations – fuzzy rules – Defuzzification – Time dependent logic – Temporal Fuzzy logic (TFC) – Fuzzy Neural Network (FANN) – Fuzzy logic controller – Fuzzification & defuzzification interface.

UNIT V APPLICATION OF FUZZY LOGIC   **9**

Application of fuzzy logic to washing machine – Vaccum cleaner – Water level controller – temperature controller- Adaptive fuzzy systems – Fuzzy filters – Sub band coding – Adaptive fuzzy frequency hoping.

REFERENCES:
1. Freeman & Skapura, "Neural Networks", Addison - Wesley, 1991
2. Zurada.J.M., "Introduction to Artificial Neural Systems", West, 1992
3. Simon Haykin, Macmillan, "Neural Networks", 1994

4. Yagnanarayana.B., "Artificial Neural Networks", Prentice Hall of India, 2006

ELECTIVE	L	T	P	C
DIGITAL CONTROL ENGINEERING	3	0	0	3

AIM:

To enhance the knowledge of student with various algorithms and techniques to apply in controllers.

OBJECTIVE:
- To study the basic digital control system design and its stability testing.
- To study the models of digital devices and systems.
- To learn about digital control algorithms.
- To study about control systems analysis using state variable methods.
- To analyse the control systems using state variable methods.

Unit I Digital Control, Signal Processing in digital control   **9**

Control sytem terminology – computer based control – control theory – classical approach to analog controller design – configuration of the basic digital control scheme – Principles of signal conversion – Basic discrete time signals – Time domain models for discrete time sytems –Transfer function models – frequency response – stability on the z-plane and the Jury Stability Criterion – Sample and Hold Systems – sampled spectra and aliasing – reconstruction of analog signals – Choice of sampling rate – Proinciples of discretization

Unit II Models of Digital Control Devices and Systems   **9**

Z – Domain Description of sampled contineous time Plants – z – domain Description of Systems with Dead–Time – Implementation of Digital Controllers – Tunable PID Controllers – Digital Temperature Control Systems – Digital Position Control Systems – Stepping Motor and Their Control – Programmable Logic Controllers.

Unit III Design of digital Control Algorithms   **9**

Z – Plane Specifications of control Systems Design – Digital Compensator Desingn using Frequency Response Plots – Digital Compensator Desingn using Root Locus Plots – z – Plane Synthesis.

Unit IV Control System analysis using state Variable Methods   **9**

Vectors and Matrices – State Variable Representations – Conversion of State Variable Models to Transfer Function – Conversion of Transfer Functions to Cononical State Variable Models – Eigen Values and Eigenvectors – State Equations – Controllability and Observability – Equivalence between Transfer Function and State Variable Representation – Multivariable Sytems.

Unit V Practical Aspects of Digital Control Algorithms   **9**

Mechanisation of control Algorithms using Microprocessors – Microprocessor Based Temperature Control Systems–Case Study – Stepping Motors and their Interfacing to Microprocessors

TOTAL HOURS: 45

Text Books

1. M. Gopal, "Digital Control and State Variable Methods Conventional Intelligent Control Systems", Tata McGraw Hill, 3rd Edition.
2. M. Gopal, "Digital Control Engineering" New Age International Publishers.

Reference Books:

1. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", Mc Graw Hill, 1995
2. B. C. Kuo, "Digital Control Systems", Oxford University Press, 2004.

ELECTIVE	L	T	P	C
DISTRIBUTED EMBEDDED COMPUTING	3	0	0	3

AIM:

As now embedded systems has to be designed with some communication facility to give interaction between themselves and multi processing systems work in a distributed environment this course on distributed embedded systems is included in the curriculum.

OBJECTIVE:

To make the student learn: distributed system concepts, JAVA programming and some design concepts related to distributed systems.

UNIT I   THE HARDWARE INFRASTRUCTURE   9

Broad Band Transmission facilities – Open Interconnection standards – Local Area Networks – Wide Area Networks – Network management – Network Security – Cluster computers.

UNIT II   INTERNET CONCEPTS   9

Capabilities and limitations of the internet – Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

UNIT III   DISTRIBUTED COMPUTING USING JAVA   9

IO streaming – Object serialization – Networking – Threading – RMI – multicasting – distributed databases – embedded java concepts – case studies.

UNIT IV   EMBEDDED AGENT   9

Introduction to the embedded agents – Embedded agent design criteria – Behaviour based, Functionality based embedded agents – Agent co-ordination mechanisms and benchmarks embedded-agent. Case study: Mobile robots.

UNIT V   EMBEDDED COMPUTING ARCHITECTURE   9

Synthesis of the information technologies of distributed embedded systems – analog/digital co-design – optimizing functional distribution in complex system design – validation and fast prototyping of multiprocessor system-on-chip – a new dynamic scheduling algorithm for real-time multiprocessor systems.

                                                    TOTAL: 45 HOURS

REFERENCES:

1. Dietel & Dietel, "JAVA how to program", Prentice Hall 1999.
2. Sape Mullender, "Distributed Systems", Addison-Wesley, 1993.
3. George Coulouris and Jean Dollimore, "Distributed Systems – concepts and design", Addison –Wesley 1988.
4. "Architecture and Design of Distributed Embedded Systems", edited by Bernd Kleinjohann C-lab, Universitat Paderborn, Germany, Kluwer Academic Publishers, Boston, April 2001, 248 pp.