VINAYAKA MISSIONS UNIVERSITY, SALEM
TAMILNADU, INDIA.

FACULTY OF ENGINEERING & TECHNOLOGY

SCHOOL OF ELECTRONIC SCIENCES

M.E- APPLIED ELECTRONICS

PART TIME

AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY, PAIYANOOR

&

V.M.K.V. ENGINEERING COLLEGE, SALEM

CHOICE BASED CREDIT SYSTEM

2012 REGULATION
### I SEMESTER

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<th>S.No.</th>
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### VI SEMESTER

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AIM:
Mathematics is fundamental for any field of technology. The aim of the subject is to impart essential mathematical topics for the PG courses in Electronics and Communication Engineering Department.

OBJECTIVE:
- To understand the concepts of fuzzy logic.
- To make the student learn different matrix methods and some of the applications.
- To understand the concepts of random variables.
- To make the student learn dynamic programming and their applications.
- To understand the concepts of different queuing models.

UNIT I: FUZZY LOGIC
Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II: MATRIX THEORY

UNIT III: ONE DIMENSIONAL RANDOM VARIABLES
Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform,
Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV: DYNAMIC PROGRAMMING

UNIT V: QUEUEING MODELS

REFERENCES:

TOTAL: 60 HOURS
AIM:

The aim of the course is to teach students to use digital signal processors such as the TMS320C6xxx to perform real-time DSP on real signals.

OBJECTIVE:

This course brings together some of the theory and understanding you have gained in several other lecture courses and lets you apply that theory in solving the type of problem which might be encountered by a DSP engineer in industry.

UNIT I: FUNDAMENTALS OF PROGRAMMABLE DSP’S


UNIT II: TMS320C5X PROCESSOR

Architecture – Assembly Language syntax- Addressing modes- Assembly language Instructions – pipeline structure, Operation – Block diagram of DSP Starter kit – Application Programs for processing real time signals.

UNIT III: TMS320C3X PROCESSOR

Architecture – Data formats – Addressing modes – Groups of addressing modes – Instruction sets – Operation – Block diagram of DSP starter kit – Application, Programs for processing real time systems – Generating and finding the sum of series, Convolution of two sequences, Filter design.

UNIT IV: ADSP PROCESSORS

Architecture of ADSP-21XX and ADSP – 210XX series of DSP processors – Addressing modes and Assembly language instructions – Applications programs – Filter design, FFT calculation- Blackfin DSP Processor

UNIT V: ADVANCED PROCESSORS


TOTAL: 60 HOURS

TEXT BOOK:


REFERENCE BOOKS:
1. User guides Texas Instrumentation, Analog Devices, Motorola.
AIM:

Learning design of digital circuits is a fundamental necessity for designing embedded systems. This subject provides necessary instruments to achieve that goal.

OBJECTIVE:

To make the student learn: theory of logic and logic functions, design of digital circuits, and an introduction to VHDL language.

1. ADVANCED TOPICS IN BOOLEAN ALGEBRA

   Shannon's expansion theorem, Consensus theorem, Octal designation, Run measure, INHIBIT / INCLUSION / AOI / Driver / Buffer gates, Gate expander, Reed Muller expansion, Synthesis of multiple output combinational logic circuits by product map method, Design of static hazard free and dynamic hazard free logic circuits.

2. THRESHOLD LOGIC

   Linear separability, Unateness, Physical implementation, Dual comparability, reduced functions, various theorems in threshold logic, Synthesis of single gate and multigate threshold Network.

3. SYMMETRIC FUNCTIONS

   Elementary symmetric functions, partially symmetric and totally symmetric functions, Mc Cluskey decomposition method, Unity ratio symmetric ratio functions, Synthesis of symmetric function by contact networks.

4. SEQUENTIAL LOGIC CIRCUITS

   Mealy machine, Moore machine, Trivial / Reversible / Isomorphic sequential machines, State diagrams, State table minimization, Incompletely specified sequential machines, State assignments, Design of synchronous and asynchronous sequential logic circuits working in the fundamental mode and pulse mode, Essential hazards Unger's theorem.

5. PROGRAMMABLE LOGIC DEVICES

   Basic concepts, Programming technologies, Programmable Logic Element (PLE), Programmable Logic Array (PLA), Programmable Array Logic (PAL), Structure of Standard PLD's, Complex PLD's (CPLD). System Design Using PLD's - Design of combinational and sequential circuits using PLD's, Programming PAL device using PALASM, Design of state machine using Algormic State Machines (ASM) chart as a design tool. Introduction To Field Programmable Gate Arrays - Types of FPGA, Xilinx XC3000 series, Logic Cell array (LCA), Configurable Logic Blocks (CLB) Input/Output Block (IOB)- Programmable Interconnect Point (PIP), Introduction to Actel ACT2 family and Xilinx XC4000 families, Design examples.

Total No of periods: 45

References:
AIM:
This course aims to provide students with an understanding of digital image processing techniques, including image reconstruction and restoration, segmentation and enhancement, also colour and morphological image processing techniques.

OBJECTIVE:
Upon successful completion of this course, students should be able to understand all types of image processing techniques.

UNIT I: INTRODUCTION TO IMAGE PROCESSING SYSTEMS & IMAGE TRANSFORMS

Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Applications of Digital image processing

Introduction, Need for transform, Image transforms, Fourier transform, 2 D Discrete Fourier transform and its transforms, Importance of phase, Walsh transform, Hadamard transform, Haar transform, slant transform Discrete cosine transform, KL transform, singular value decomposition, Radon transform, comparison of different image transforms.

UNIT II: IMAGE ENHANCEMENT & IMAGE RESTORATION

Introduction to image enhancement, Enhancement in spatial domain, enhancement through point operation, Types of point operation, Histogram manipulation, Linear Gray level transformation, Nonlinear Gray level transformation, Local or neighbourhood operation, Median filter, Image sharpening, Bit plane slicing, Image enhancement in the frequency domain.

Introduction to Image restoration, Image degradation, Types of image blur, Classification of image restoration techniques, Image restoration model, Linear and Nonlinear image restoration techniques, Blind deconvolution

UNIT III: IMAGE SEGMENTATION AND IMAGE COMPRESSION

Introduction to image segmentation, Classification of segmentation techniques, Region approach to image segmentation, clustering techniques, Image segmentation based on thresholding, Edge based segmentation, Edge detection and linking, Hough transform, Active contour

Introduction, Need for image compression, Redundancy in images, Classification of redundancy in images, image compression scheme, Classification of image compression schemes, Fundamentals of information theory, Run length coding, Shannon – Fano coding, Huffman coding, Arithmetic coding,
Predictive coding, Transformed based compression, Image compression standard, Wavelet-based image compression

UNIT IV: COLOUR IMAGE PROCESSING

Introduction, Light and colour, colour formation, Human perception of colour, colour model, The chromaticity diagram, colour image quantization, Histogram of colour image, colour image filtering, Gamma correction of a colour image, colour image segmentation.

UNIT V: MORPHOLOGICAL IMAGE PROCESSING

Preliminaries-Dilation & Erosion, Opening & Closing, Hit or Miss Transformation, Basic Morphological Algorithms, Extension to Gray scale Images.

TOTAL: 45 HOURS

REFERENCE BOOKS:


AIM:

To develop an awareness of the requirements for IC technology. Understand how device miniaturization has led to improved device performance and the potential limits to this process.

OBJECTIVES:

- The aim of this course is to describe the design, technology and manufacture of MOS integrated circuits and future nanoscale electron devices.
- It will provide a firm foundation for those wishing to pursue careers in applications or in research/development in the field of semiconductor devices/circuits.

UNIT I MOS TRANSISTOR THEORY AND PROCESS TECHNOLOGY 9

NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II INVERTERS AND LOGIC GATES. 9

NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics, switching times, Super buffers, Driving large capacitance loads, CMOS logic structures, Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III CIRCUIT CHARACTERIZATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing, Scaling.

UNIT IV VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN. 9


UNIT V VERILOG HARDWARE DESCRIPTION LANGUAGE 9

Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modeling, data flow modeling, behavioral modeling, task & functions, Test Bench.

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

TEXT BOOK:


REFERENCES

List of Experiments

Experiments based on Advanced Digital Signal Processing
Sampling of signals, study of aliasing error, multi-rate sampling
Adaptive filter design
Spectral Analysis of signals
AIM:

To provide the background and the methods for the understanding of the operation of basic analogue CMOS cells, and how to design common functions.

OBJECTIVE:

- To study the basic models of IC active devices
- To study the circuit configuration for linear ICs
- To study the operational amplifiers construction and its response analysis
- To study the analog multipliers, PLL and noise calculation in devices
- To study the analog design with MOS technology.

UNIT I: MODELS FOR INTEGRATED CIRCUIT ACTIVE DEVICES  

UNIT II: CIRCUIT CONFIGURATION FOR LINEAR IC  

UNIT III: OPERATIONAL AMPLIFIERS  
Applications of operational amplifiers, Deviations from ideality in real operational amplifiers, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise.

UNIT IV: ANALOG MULTIPLIER AND PLL  
Precision Rectification- Analog Multipliers employing the bipolar transistor, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits, Noise in Integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature.

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY  
MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Basic Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers.

TOTAL: 45 HOURS

TEXT BOOK:

REFERENCE BOOKS:
1. Behzad Razavi, “Principles of data conversion system design”, S.Chand and company Ltd, 2000
AIM:
To provide the basic concepts of embedded systems and its hardware, software utilization towards real time applications.

OBJECTIVE:
- To study the basic hardware components available for embedded system.
- To study ISR and different architectures available.
- To study in detail about RTOS environment.
- To study various debugging strategies.
- To study the real time implementation procedures using RTOS.

UNIT I INTRODUCTION 9
Examples of Embedded Systems, Typical hardware, Terminology, Gates, Timing diagrams, Memory, Microprocessors, buses, direct memory access, interrupts, built-ins on the microprocessor, conventions used on schematics.

UNIT II INTERRUPTS & SOFTWARE ARCHITECTURES 9
Interrupt basics, shared data problem, interrupt latency; Software architectures – Round Robin, Round Robin with interrupts, function queue scheduling architecture, real time operating system architecture, selecting an architecture.

UNIT III - INTRODUCTION TO REAL TIME OPERATING SYSTEMS AND OPERATING SYSTEM SERVICES 9
Tasks and task states, Tasks and data, semaphores and shared data, Message queues, Mailboxes and pipes, Timer functions, Events, Memory management, Interrupt routines in an RTOS environment

UNIT IV EMBEDDED SOFTWARE DEVELOPMENT AND DEBUGGING TECHNIQUES 9
The compilation process, native versus cross compilers, Libraries – run time libraries, writing a library, using alternative libraries, using a standard library, Porting kernels, Downloading. Debugging techniques, Emulation techniques,

UNIT V BASIC DESIGN USING A REAL TIME OPERATING SYSTEM & DESIGN EXAMPLES 9
Principles, Encapsulating semaphores and queues, Hard time scheduling considerations, saving memory space and power. 
Embedded system design and coding for an automatic chocolate vending machine, case study of an embedded system for an adaptive cruise control system in a car, case study of an embedded system for a smart card.

TUTORIAL: 15 HOURS
TOTAL: 60 HOURS

TEXT BOOKS:

REFERENCE BOOKS:
AIM:
To provide the knowledge on Parallel Computing and its architectures and processing,

OBJECTIVES:
- At the end of this course the student will know various parallel processing applications and their performance towards real time computing.
- To impart knowledge on scalable architectures and the performances.

UNIT I- THEORY OF PARALLELISM, PARTITIONING AND SCHEDULING 9
Parallel Computer models: The state of computing, Multiprocessors and Multicomputers, Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks.
Program and network properties: Conditions of parallelism, Program partitioning and scheduling, program flow mechanisms, System interconnect architectures.

UNIT II- SCALABLE PERFORMANCES & HARDWARE TECHNOLOGIES 9
Principles of scalable performance: Performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.
Processor and memory hierarchy: Advanced processor technology, Superscalar and vector processors, memory hierarchy technology, virtual memory technology.

UNIT III- MEMORY ORGANIZATIONS & PIPELINING 9
Bus cache and shared memory: backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.
Pipelining: Linear and non-Linear Pipeline processors-Instruction pipeline design and Arithmetic pipeline design.

UNIT IV- PARALLEL & SCALABLE ARCHITECTURES 9
Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V-SOFTWARE & PARALLEL PROCESSING 9
Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL: 45 HOURS

TEXT BOOKS:

REFERENCE BOOKS:
AIM:
To learn all parts of communication software in layered architecture.

OBJECTIVE:
- To study the basics on computer networks and its protocols
- To study the transport layer protocol of OSI model.
- To learn about network layer of OSI model.
- To study data link and MAC layer of OSI model.
- To learn about network security in computer networks.

UNIT I OVERVIEW OF COMPUTER NETWORKS AND APPLICATION LAYER PROTOCOLS
An introduction to internet - An overview of circuit switching - Packet switching and message switching - Routing in data networks - Access networks and physical media - Protocol; layers - Comparison of OSI and Internet protocol stack - Internet backbones - Network access points and ISPs, Application layer protocols - Service provided by the Internet transport protocols – Network applications: www - Overview of HTTP - HTTP message format - User server interaction – Web caches FTP - FTP commands and replies - Electronic mail in the internet - SMPT, MIME – Mail access protocols - POP3 DNS - Introduction to socket programming with TCP and UDP.

UNIT II TRANSPORT LAYER PROTOCOLS
Transport layer services and principles - Relationship between transport and network layers - Overview of transport layer in the internet - Multiplexing and demultiplexing applications connectionless and connection oriented transports - Principles of reliable data transfer – Principles of congestion control.

UNIT III NETWORK LAYER

UNIT IV DATA LINK AND MAC LAYER
Data link layer services and adapters - Error detection and correction techniques – Multiple Access protocols and LANs - LAN addresses and ARP - Ethernet - Hubs - Bridges and Switches PPP- ATM- X.2.5 and Frame relay.

UNIT V NETWORK SECURITY AND MULTIMEDIA
Networks security - Principles of cryptography - Authentication - Integrity - Key distribution and certification - Secure Email - Internet commerce - Network layer security - Multimedia networking application - Streaming stored audio and video - Internet phone - Case study - RTP.

TOTAL HOURS: 45

REFERENCE BOOKS:
AIM: To provide the programming knowledge on embedded processors

List of Experiments:
1. Board development using 8051 microcontroller
2. Assembly and High level language programs for 8051 - ports – timers -Seven Segment display – UART – LCD interface
3. RTOS – Simple task creation, Round Robin Scheduling, Preemptive scheduling, Semaphores, Mailboxes.
4. Assembly and High level language programs for R8C - ports – timers -Seven Segment display – UART – LCD interface – Stepper Motor control
5. Assembly and High level language programs for MSP 430 - ports – timers - Seven Segment display – UART – LCD interface – Stepper Motor control
AIM:
To make the student learn the fundamentals of ASIC and its design methods.

OBJECTIVE:
- To study the basics of ASIC and its cell design
- To learn about Programmable ASIC I/O Cells.
- To learn about various ACIC programmable logic cells.
- To study the simulation, synthesis and testing of ASIC.
- To study about ASIC construction, floor planning, placement and routing.

UNIT I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN
9
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance - Logical effort –Library cell design - Library architecture

UNIT II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS
9
Programmable ASIC I/O CELLS
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY
9

UNIT IV LOGIC SYNTHESIS, SIMULATION AND TESTING
9
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING
9
System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

TOTAL HOURS: 45

REFERENCES:
AIM:
The aim of this course is to develop and deploy advances in measurement science to safely increase the versatility, autonomy, and rapid re-tasking of intelligent robots and automation technologies.

OBJECTIVE:
At the end of this course student will infer some knowledge regarding advanced robotics and automation.

UNIT I INTRODUCTION
Geometric configuration of robots - manipulators - drive systems - internal and external sensors - end effectors - control systems - robot programming languages and applications - Introduction to robotic vision.

UNIT II ROBOT ARM KINEMATICS
Direct and Inverse Kinematics - rotation matrices - composite rotation matrices - Euler angle representation - homogeneous transformation - Denavit Hattenberg representation and various arm configurations.

UNIT III ROBOT ARM DYNAMICS

UNIT IV ROBOT APPLICATIONS

UNIT V ASSEMBLY AND INSPECTION
Assembly and robotic assembly automation – Parts presentation methods – assembly operation – Compliance and the Remote Center Compliance(RCC) device – Assembly system Configurations – Adaptable, Programmable assembly system – Designing for robotic assembly – Inspection automation.

TOTAL HOURS: 45

REFERENCES:
AIM
The purpose of Video Processing course is to cover the fundamentals of digital video signal generation and further processing over the communication systems.

OBJECTIVE
To learn the basic concepts of video processing
To learn about the various methodologies for motion estimation
To learn the basic concepts of coding systems
To understand about the waveform based video coding techniques
To understand about the content dependent and scalable video coding techniques

UNIT I VIDEO FORMATION, PERCEPTION AND REPRESENTATION  9

UNIT II TWO-DIMENSIONAL MOTION ESTIMATION  9
General Methodologies, Pixel-Based Motion Estimation., Block Matching Algorithm, Mesh-based Motion estimation, Global Motion Estimation, Region –Based Motion Estimation, Multiresolution Motion Estimation, Application of Motion Estimation in Video Coding. Feature-based Motion Estimation.

UNIT III FOUNDATONS OF VIDEO CODING  9
Overview of Coding Systems, Basic Notions in Probability and Information Theory, Information Theory for Source Coding, Binary Encoding, Scalar Quantization , Vector Quantization.

UNIT IV WAVEFORM-BASED VIDEO CODING  9
Block-Based Transform Coding, Predictive Coding, Video Coding Using Temporal Prediction and Transform Coding.

UNIT V CONTENT-DEPENDENT & SCALABLE VIDEO CODING  9
Two-Dimensional Shape Coding, Texture coding for Arbitrarily Shaped Regions, Joint Shape & Texture Coding, Region-Based Video Coding, Object-based Video Coding. Basic Modes of Scalability, Object Based Scalability, Wavelet-transform Based Coding.

TOTAL HOURS: 45

TEXT BOOKS:

REFERENCES:
AIM:
This course aims to provide the student to apply engineering knowledge and specialist techniques to prevent or to reduce the likelihood or frequency of failures.

OBJECTIVE:
The students will be able to understand the ways in which product fail, the effects of failure and aspects of design, manufacture, maintenance and use which affect the likelihood of failure.

UNIT I PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE
Statistical distribution, statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference, Safety margin and loading roughness on reliability.

UNIT II RELIABILITY PREDICTION, MODELLING AND DESIGN
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design, software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV RELIABILITY TESTING AND ANALYSIS
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V MANUFACTURE AND RELIABILITY MANAGEMENT
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

TOTAL HOURS: 45

REFERENCES:
### AIM:

To understand different electromagnetic Interference problems occurring in Intersystem and in inter system and their possible mitigation techniques in Electronic design.

### OBJECTIVES:

- To understand EMI Sources, EMI problems and their solution methods in PCB level / Subsystem and system level design.
- To measure the emission immunity level from different systems to couple with the prescribed EMC standards.

### UNIT I EMI/EMC CONCEPTS

EMI- EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

### UNIT II EMI COUPLING PRINCIPLES

Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differential mode coupling; Near field cable to cable coupling, cross talk; Field to cable coupling; Power mains and Power supply coupling.

### UNIT III EMI CONTROL TECHNIQUES

Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

### UNIT IV EMC DESIGN OF PCBS

Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

### UNIT V EMI MEASUREMENTS AND STANDARDS

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

### TOTAL HOURS: 45

### REFERENCES:

AIM:
To expose students to the advanced digital signal processing systems for VLSI and associated EDA Tools.

OBJECTIVE:
At the end of this course the student will be able knowing methods and techniques for implementation of DSP systems.

UNIT I  INTRODUCTION TO DSP SYSTEMS  9
Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Longest path Matrix algorithm; Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

UNIT II  RETIMING  9
Retiming - definitions and properties; Unfolding – an algorithm for Unfolding, properties of unfolding, sample period reduction and parallel processing application; Algorithmic strength reduction in filters and transforms – 2-parallel FIR filter, 2-parallel fast FIR filter, DCT algorithm architecture transformation, parallel architectures for rank-order filters, Odd- Even Merge- Sort architecture, parallel rank-order filters.

UNIT III  FAST CONVOLUTION  9

UNIT IV  BIT-LEVEL ARITHMETIC ARCHITECTURES  9
Scaling and roundoff noise- scaling operation, roundoff noise, state variable description of digital filters, scaling and roundoff noise computation, roundoff noise in pipelined first-order filters; Bit-Level Arithmetic Architectures- parallel multipliers with sign extension, parallel carry-ripple array multipliers, parallel carry-save multiplier, 4x 4 bit Baugh-Wooley carry-save multiplication tabular form and implementation, design of Lyon’s bit-serial multipliers using Horner’s rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner’s rule for precision improvement.

UNIT V  PROGRAMMING DIGITAL SIGNAL PROCESSORS  9
Numerical Strength Reduction – subexpression elimination, multiple constant multiplications, iterative matching. Linear transformations; Synchronous, Wave and asynchronous pipelining- synchronous pipelining and clocking styles, clock skew in edge-triggered single-phase clocking, two-phase clocking, wave pipelining, asynchronous pipelining bundled data versus dual rail protocol; Programming Digital Signal Processors – general architecture with important features; Low power Design – needs for low
power VLSI chips, charging and discharging capacitance, short-circuit current of an inverter, CMOS leakage current, basic principles of low power design.

TOTAL HOURS: 45

REFERENCES:
AIM
To produce the knowledge on cyber security essentials

OBJECTIVE
- To study the cyber security fundamentals
- To study the various techniques on attack and exploitation
- To study in detail about malicious code
- To study about defense and analysis techniques

UNIT I CYBER SECURITY FUNDAMENTALS


UNIT II ATTACKER TECHNIQUES AND MOTIVATIONS

Antiforensics – Tunneling techniques – Fraud Techniques - Threat Infrastructure.

UNIT III EXPLOITATION

Techniques to gain a foot hold – Misdirection, Reconnaissance, and disruption methods.

UNIT IV MALICIOUS CODE


UNIT V DEFENSE AND ANALYSIS TECHNIQUES


TOTAL HOURS: 45

TEXT BOOK

REFERENCE BOOKS
AIM:
Main aim of this course is to make the students understand in identifying and analyzing the requirements that a distributed multimedia application may enforce on the communication network.

OBJECTIVE:
At the end of this course students have knowledge in distributing multimedia application over the communication network.

UNIT I MULTIMEDIA NETWORKING
Digital sound, video and graphics, basic multimedia networking, multimedia characteristics, evolution of Internet services model, network requirements for audio/video transform, multimedia coding and compression for text, image, audio and video.

UNIT II BROAD BAND NETWORK TECHNOLOGY
Broadband services, ATM and IP, IPV6, High speed switching, resource reservation, Buffer management, traffic shaping, caching, scheduling and policing, throughput, delay and jitter performance.

UNIT III MULTICAST AND TRANSPORT PROTOCOL
Multicast over shared media network, multicast routing and addressing, scaping multicast and NBMA networks, Reliable transport protocols, TCP adaptation algorithm, RTP, RTCP.

UNIT IV MEDIA - ON – DEMAND
Storage and media servers, voice and video over IP, MPEG over ATM/IP, indexing synchronization of requests, recording and remote control.

UNIT V APPLICATIONS
MIME, Peer-to-peer computing, shared application, video conferencing, centralized and distributed conference control, distributed virtual reality, light weight session philosophy.

TOTAL HOURS: 45

REFERENCES:
AIM:
This course is intended to introduce the student to learn about Device Modeling- Various types of analog systems- CMOS amplifiers and Comparators.

OBJECTIVE:
- To demonstrate an understanding of MOS terminal characteristics and capacitive effects.
- To create integrated circuit layouts showing an awareness of the underlying process technology and layout parasitic as well as their impact on circuit performance.

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING
Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOS Transistor-Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage BiCMOS Op-Amp Design- Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT-MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING
Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks-Floating-Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER-AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT

TOTAL HOURS: 45

REFERENCES:
AIM:

As there is always a need for power efficient circuits and devices, this course explains the methods for low power VLSI design.

OBJECTIVE:

At the end of this course, the student will be able to design Low power CMOS designs, for digital circuits.

UNIT I

9
Introduction - Simulation - Power Analysis-Probabilistic Power Analysis.

UNIT II

9

UNIT III

9

UNIT IV

9

UNIT V

9

TOTAL HOURS: 45

REFERENCES:

AIM:
The aim of this course is to give the students knowledge about the usage of computer for the design of VLSI circuits. It also provides the flow of process involved and how design can be simulated.

OBJECTIVE:
At the end of this course the student will have knowledge in using computer simulation software for designing the VLSI circuits.

UNIT I

UNIT II
Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms - partitioning

UNIT III
Floorplanning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV
Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V
High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations.

TOTAL HOURS: 45

REFERENCES:
AIM:

The aim of this course is provide an introduction of an advanced element of learning in the field of wireless communication and also expose the students to the concepts of wireless devices and mobile computing.

OBJECTIVE:

At the end of this course the student should be able to understand the concept of mobile computing and architecture of mobile communication.

UNIT – I: WIRELESS TRANSMISSION


UNIT – II: TELECOMMUNICATION SYSTEM

GSM- DECT- Tetra- UMTS- IMT 2000- GPRS

UNIT – III: WIRELESS LAN


UNIT – IV: MOBILE NETWORK LAYER

Mobile IP- Dynamic post configuration protocol- mobile Adhoc network- DSDV- DSR- AODV- ZRP- OVMR.

UNIT – V: MOBILE TRANSPORT LAYER AND APPLICATION

TCP- WAP- Architecture- WDGP- WTLS- WTP- WSP- WML- WAE- WML script- WTA.

TOTAL HOURS: 45

TEXT BOOK


REFERENCE

AIM:

Since the concepts of real time systems and their analysis is very essential for embedded students this subject is given.

OBJECTIVE:

To make the student learn, all real time aspects of various system components, like OS, memory, communication and an introduction to reliability evaluation methods.

1. INTRODUCTION

Introduction - issues in real time computing - structure of a real time system - task classes - performance measures for real time systems - estimating program run times - task assignment and scheduling - classical uniprocessor scheduling algorithms - uniprocessor scheduling of IRIS tasks - tasks assignment - mode changes - fault tolerant scheduling.

2. PROGRAMMING LANGUAGES AND TOOLS

Language features - desired language characteristics - data typing - control structures - facilitating hierarchical decomposition - package - run-time error handling - overloading and generics - multitasking - low level programming - task scheduling - timing specifications - programming environments - run-time support – code generation.

3. REAL TIME DATABASES

Real time database - basic definition - real time Vs general-purpose database - main memory databases - transaction priorities - transaction aborts - concurrency control issues - disk scheduling algorithms - two-phase approach to improve predictability - maintaining serialization consistency - databases for hard real time systems.

4. COMMUNICATION


5. EVALUATION TECHNIQUES
Reliability evaluation techniques - reliability models for hardware redundancy - software error models – response time calculation – interrupt latency – time loading and its measurement – reducing response times – analysis of memory requirements – reducing memory loading

TOTAL HOURS: 45

TEXT BOOK:

REFERENCES:
AIM:

The use of real time operating systems has become a necessity to build complex embedded systems, this subject is provided.

OBJECTIVE:

To make the student learn fundamentals of Operating Systems, implementation aspects of real time concepts and few applications on RTOS.

UNIT I: REVIEW OF OPERATING SYSTEMS


UNIT II: OVERVIEW OF RTOS

RTOS Task and Task state - Process Synchronisation - Message queues – Mail boxes - pipes – Critical section – Semaphores – Classical synchronisation problem – Deadlocks -

UNIT III: REAL TIME MODELS AND LANGUAGES

Event Based – Process Based and Graph based Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT IV: REAL TIME KERNEL


UNIT V: RTOS APPLICATION DOMAINS


TOTAL HOURS: 45

REFERENCES:


AIM:
To make the student learn: use of C language for embedded applications, real time UML concepts, co-design methods.

OBJECTIVE:
- To study basic programming concepts
- To learn the C and assembly.
- To learn about object oriented analysis and design.
- To learn about UML and its architectures.

1. LOW LEVEL PROGRAMMING IN C 9

2. C AND ASSEMBLY 9

3. OBJECT-ORIENTED ANALYSIS AND DESIGN 9

4. UNIFIED MODELLING LANGUAGE 9

5. CASE STUDIES 9

TOTAL HOURS: 45

REFERENCES:
2. Hassan Gomma, “Designing Concurrent, Distributed, and Real-Time applications with UML.
ELECTIVE

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AIM:

To make the student learn, basics of control systems, application methods of control theory in embedded systems.

OBJECTIVE:

- To study the basic hardware of embedded control systems.
- To study the input and output devices of a system.
- To study the utilization of DAC/ADC.
- To study the functioning of serial communication devices.

1. INTRODUCTION

Controlling the hardware with software – data lines – numbering systems – address lines - ports – schematic representation – bit masking – programmable peripheral interface – switch input detection.

2. INPUT-OUTPUT DEVICES


3. D/A AND A/D CONVERSION

R 2R ladder - more on Op-Amps - virtual ground - resistor network analysis - port offsets - triangle waves analog vs digital values - ADC0809 – comparator - successive approximation - the ADC clock - ripple counter - D flip-flop - Q and NOT Q - aliasing – multiplexer - Auto port detect - recording and playing back voice - capturing analog information in the timer interrupt service routine - automatic, multiple channel analog to digital data acquisition.

4. ASYNCHRONOUS SERIAL COMMUNICATION


5. CASE STUDIES


**TOTAL HOURS: 45**

REFERENCES:

AIM:
This course is an introduction to MEMS, which also uses micro electronics. This course fulfills the need of electronic engineer who want to create MEMS devices.

OBJECTIVE:
At the end of this course, the student will have knowledge on MEMS materials, fabrication and micro sensor design.

UNIT I MEMS AND MICROSYSTEMS
Typical MEMs and Microsystems, materials for MEMS - active substrate materials- Silicon and its compounds, Silicon piezoresistors, Gallium Arsenide, quartz, polymers. Micromachining-photolithography, thin film deposition, doping, etching, bulk machining, wafer bonding, LIGA

UNIT II MICROSENSORS AND ACUATORS
Mechanical sensors and actuators – beam and cantilever, piezoelectric materials, thermal sensors and actuators- micromachined thermocouple probe, Peltier effect heat pumps, thermal flow sensors, Magnetic sensors and actuators- Magnetic Materials for MEMS, Devices

UNIT III MICRO OPTO ELECTRO MECHANICAL SYSTEMS
Fundamental principle of MOEMS technology, light modulators, beam splitter, microlens, digital micromirror devices, light detectors, optical switch

UNIT IV MICROFLUIDIC SYSTEMS
Microscale fluid, expression for liquid flow in a channel, fluid actuation methods, dielectrophoresis, microfluid dispenser, microneedle, micropumps-continuous flow system

UNIT V APPLICATIONS OF MEMS
Drug delivery, micro total analysis systems (MicroTAS) detection and measurement methods, microsystem approaches to polymerase chain reaction (PCR), DNA hybridization, Electronic nose, Bio chip

TOTAL HOURS: 45

REFERENCE BOOK:
AIM:
To provide the knowledge on entire RF System design and also the devices, blocks used for the RF design.

OBJECTIVE:
- This course gives the students with practical knowledge on RF transceiver system design for wireless communications.
- This course provides systematic design methods of receivers and transmitters used in communication systems and along with their details of devices.

UNIT I CMOS PHYSICS, TRANSCEIVER SPECIFICATIONS AND ARCHITECTURES

UNIT II IMPEDANCE MATCHING AND AMPLIFIERS

UNIT III FEEDBACK SYSTEMS AND POWER AMPLIFIERS

UNIT IV PLL AND FREQUENCY SYNTHESIZERS
PLL: Linearised Model –Noise properties –Phase detectors –Loop filters and Charge pumps Frequency Synthesizers: Integer-N frequency synthesizers –Direct Digital Frequency synthesizers

UNIT V MIXERS AND OSCILLATORS

TOTAL HOURS: 45

TEXT BOOKS:
AIM:

To enhance the knowledge of student with various algorithms and techniques to apply in controllers.

OBJECTIVE:

- To study the basic digital control system design and its stability testing.
- To study the models of digital devices and systems.
- To learn about digital control algorithms.
- To study about control systems analysis using state variable methods.
- To analyse the control systems using state variable methods.

Unit I Digital Control, Signal Processing in digital control


Unit II Models of Digital Control Devices and Systems


Unit III Design of digital Control Algorithms


Unit IV Control System analysis using state Variable Methods


Unit V Practical Aspects of Digital Control Algorithms

Mechanisation of control Algorithms using Microprocessors – Microprocessor Based Temperature Control Systems–Case Study – Stepping Motors and their Interfacing to Microprocessors
TOTAL HOURS: 45

Text Books

Reference Books:
AIM:
To provide in depth knowledge to students about the artificial neural networks and also Fuzzy Logic as well as application of it.

OBJECTIVE:
- To make the student learn to improve their skills over artificial neural network and their application.
- To make the student learn to understand the concepts of fuzzy logic and their application.

UNIT I FUNDAMENTALS OF ANN

UNIT II ANN ALGORITHM

UNIT III APPLICATION OF ANN

UNIT IV INTRODUCTION TO FUZZY LOGIC

UNIT V APPLICATION OF FUZZY LOGIC

TOTAL HOURS: 45

REFERENCE BOOKS: